TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

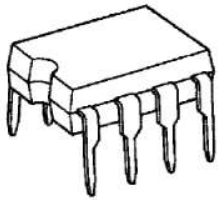
TA75458P, TA75458S, TA75458F, TA75458FB

DUAL OPERATIONAL AMPLIFIER

FEATURES

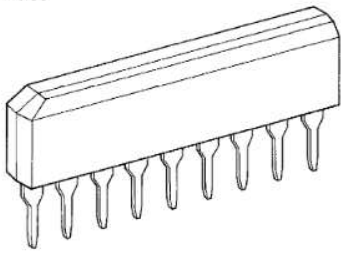
- Pair of Internally Compensated High Performance Amplifier
- No Frequency Compensation Required
- No Latch-up
- Short Circuit Protection
- Side Common Mode and Differential Voltage Range
- Low Power Consumption

TA75458P



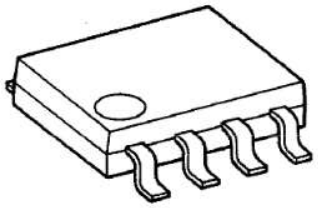
DIP8-P-300-2.54A

TA75458S



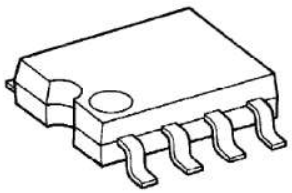
SIP9-P-2.54A

TA75458F



SOP8-P-225-1.27

TA75458FB



SOP8-P-225-1.27B

Weight
DIP8-P-300-2.54A : 0.5g (Typ.)
SIP9-P-2.54A : 0.9g (Typ.)
SOP8-P-225-1.27 : 0.1g (Typ.)
SOP8-P-225-1.27B : 0.1g (Typ.)

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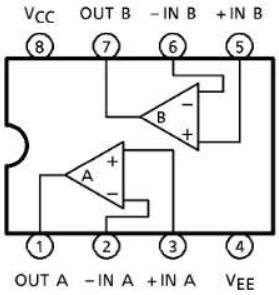
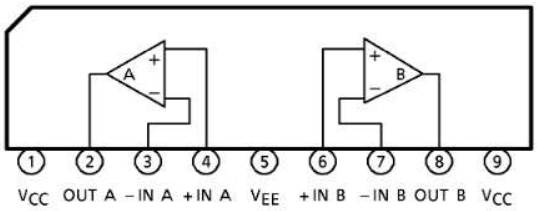
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

PIN CONNECTION (TOP VIEW)

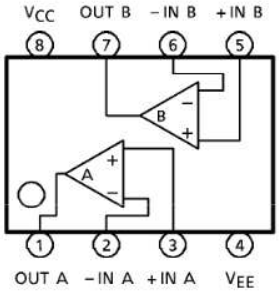
TA75458P



TA75458S



TA75458F



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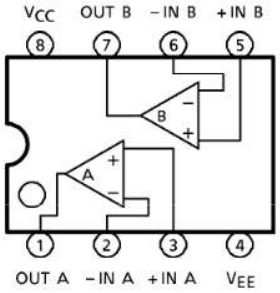
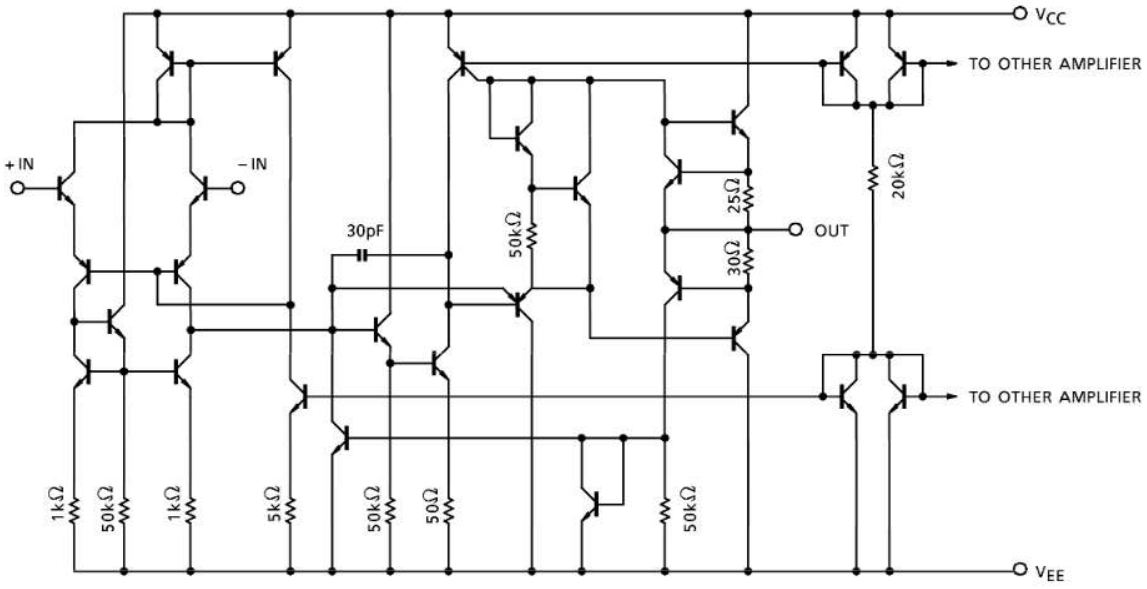


EQUIVALENT CIRCUIT



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- The information contained herein is subject to change without notice.

MAXIMUM RATINGS (Ta = 25°C)

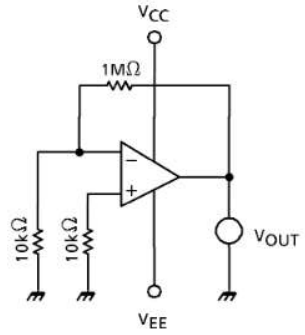
CHARACTERISTIC	SYMBOL	TA75458P	TA75458S	TA75458F TA75458FB	UNIT
Supply Voltage	V_{CC}, V_{EE}	+ 18, − 18	+ 18, − 18	+ 18, − 18	V
Differential Input Voltage	DV_{IN}	± 30	± 30	± 30	V
Input Voltage	V_{IN}	V_{CC}~V_{EE}	V_{CC}~V_{EE}	V_{CC}~V_{EE}	V
Power Dissipation	P_D	500	400	240	mW
Operating Temperature	T_{opr}	− 40~85	− 40~85	− 30~75	°C
Ambient Temperature	T_{stg}	− 55~125	− 55~125	− 55~125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, V_{EE} = − 15V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage		V_{IO}	1	$R_g \leqq 10k\Omega$	—	1	5	mV
Input Offset Current		I_{IO}	2		—	20	200	nA
Input Bias Current		I_I	2		—	80	500	nA
Common Mode Input Voltage		CMV_{IN}	3		± 12	± 13	—	V
Maximum Output Voltage		V_{OM}	4	$R_L = 10k\Omega$	± 12	± 14	—	V
		V_{OMR}	4	$R_L = 2k\Omega$	± 10	± 13	—	
Source Current		I_{source}	4		—	20	—	mA
Sink Current		I_{sink}	4		—	20	—	mA
Differential Input Impedance	Parallel Input Resistance	Z_{Di}	—	f = 20Hz Open Loop	0.3	1.0	—	MΩ
	Parallel Input Capacitance	C_i	—		—	6.0	—	pF
Output Impedance		Z_o	—	f = 20Hz	—	75	—	Ω
Voltage Gain (Open Loop)		G_V	7	V_{OUT} = ± 10V, $R_L = 2k\Omega$	86	100	—	dB
Common Mode Input Signal Rejection Ratio		CMRR	3	f = 100Hz	70	90	—	dB
Supply Voltage Rejection Ratio		SVRR	1	$R_g \leqq 10k\Omega$	—	30	150	μV / V
Power Bandwidth		f_W	—	G_V = 1, $R_L = 2k\Omega$ $V_{OUT} = 20V_{p-p}$	—	14	—	kHz
Slew Rate		SR	6	G_V = 1, $R_L = 2k\Omega$	—	0.8	—	V / μs
Unity Gain Cross Frequency		f_T	7	Open Loop	—	1.1	—	MHz
Power Dissipation		P_D	5	V_O = 0V	—	70	170	mW
Input Offset Voltage Drift		$\Delta V_{IO} / \Delta T$	1	$R_g \leqq 10k\Omega$, Ta = − 30~75°C	—	—	50	μV / °C
Supply Current		I_{CC}, I_{EE}	5		—	2.3	5.6	mA

TEST CIRCUIT

(1) V_{IO}, $\Delta V_{IO} / \Delta T$, SVRR



$V_{IO} = V_{OUT} / 100$ (V)

$\Delta V_{IO} / \Delta T = \{V_{IO}(25°C) - V_{IO}(-30°C)\} / 55$ (V / °C)

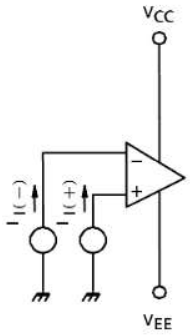
$\Delta V_{IO} / \Delta T = \{V_{IO}(75°C) - V_{IO}(25°C)\} / 50$ (V / °C)

SVRR = $(V_{IO1} - V_{IO2}) / 5$ (μV / V)

V_{IO1} : V_{CC}, AT $V_{EE} = \pm 17.5$V

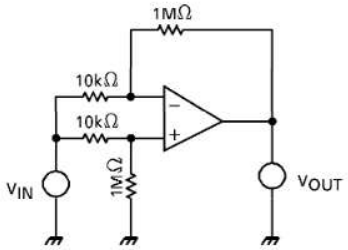
V_{IO2} : V_{CC}, At $V_{EE} = \pm 12.5$V

(2) I_I, I_{IO}



$I_{IO} = |I_{I(+)} - I_{I(-)}|$

(3) CMV_{IN}, CMRR

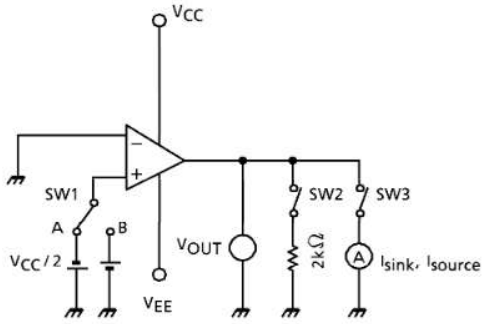


CMV_{IN} : $V_{OUT} = \pm 1$V (DC)
V_{IN} = MEASURE

CMRR : RATIO OF G_{diff} vs G_{CM}

$$CMRR = 20\ell og\frac{G_{diff}}{G_{CM}} \text{ (dB)}$$

(4) V_{OM}, V_{OMR}, I_{sink}, I_{source}



V_{OM} (+) : SW1 IS SIDE B, SW2 OFF, SW3 OFF

V_{OM} (−) : SW1 IS SIDE A, SW2 OFF, SW3 OFF

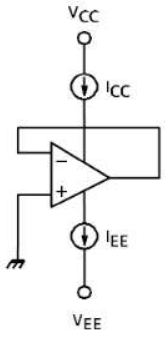
V_{OMR} (+) : SW1 IS SIDE B, SW2 ON, SW3 OFF

V_{OMR} (−) : SW1 IS SIDE A, SW2 ON, SW3 OFF

I_{sink} : SW1 IS SIDE A, SW2 OFF, SW3 ON

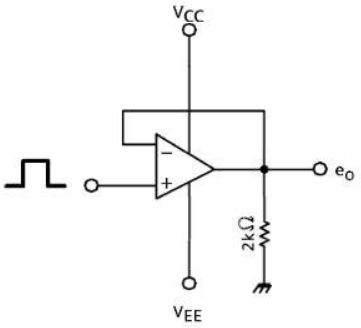
I_{source} : SW1 IS SIDE B, SW2 OFF, SW3 ON

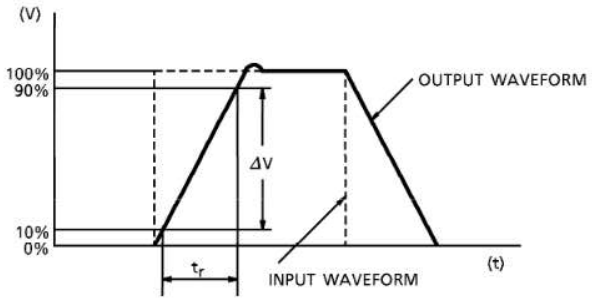
(5) I_{CC}, I_{EE}, P_D



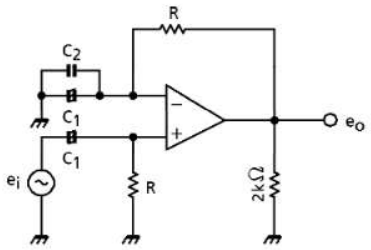
$$P_D = V_{CC} \cdot I_{CC} + V_{EE} \cdot I_{EE} \text{ (W)}$$

(6) SR





(7) G_V, f_T



G_V

$R \gg 1/WC_1$

C_1 : COUPLING CONDENSER

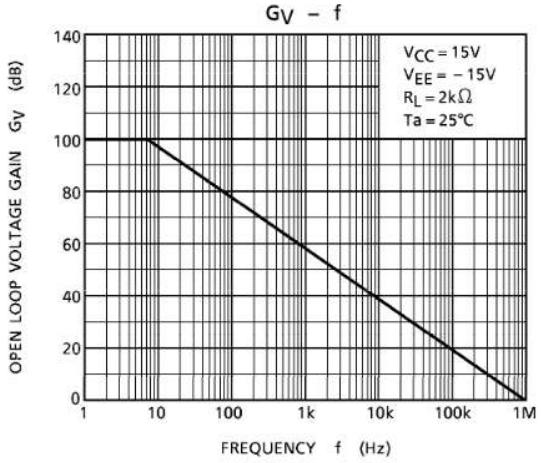
C_2 : HIGH FREQUENCY BYPASS CONDENSER
0.1μF

$G_V = 20\ell og\ e_o / e_i$ (dB)

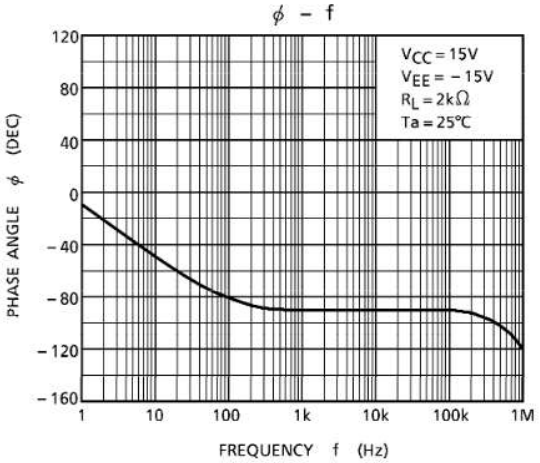
f_T INPUT FREQUENCY AT $e_i = e_o$

CHARACTERISTICS

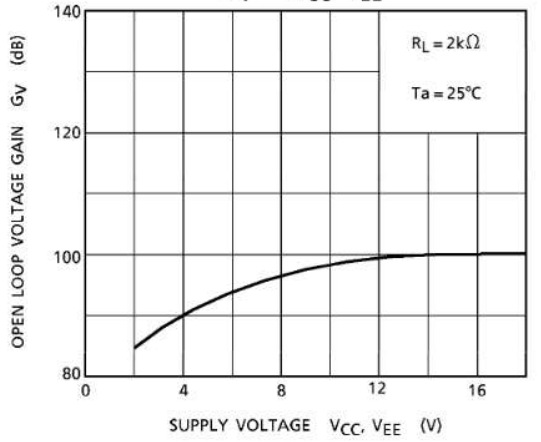
G_V – f



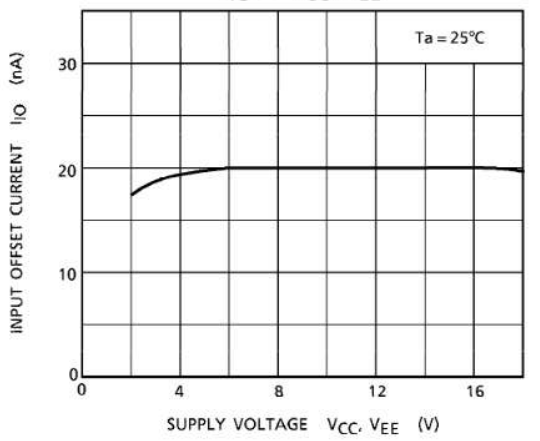
ϕ – f



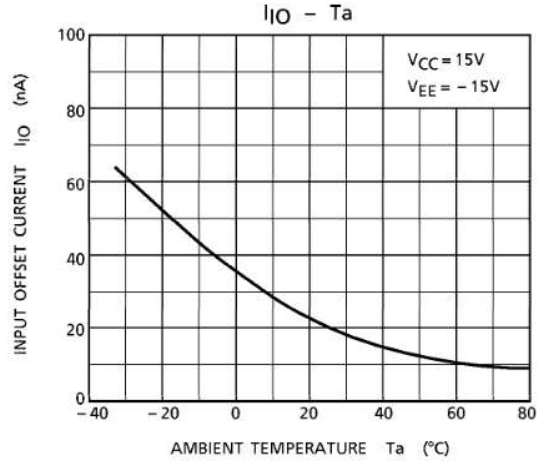
G_V – V_{CC}, V_{EE}



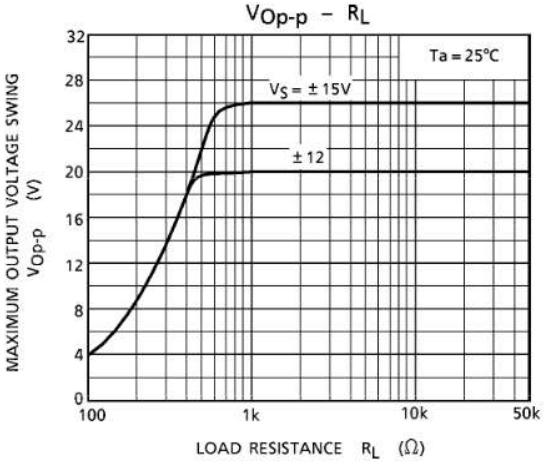
I_{IO} – V_{CC}, V_{EE}



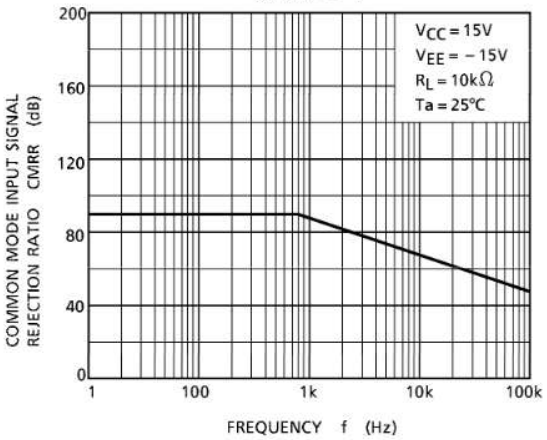
I_{IO} – Ta



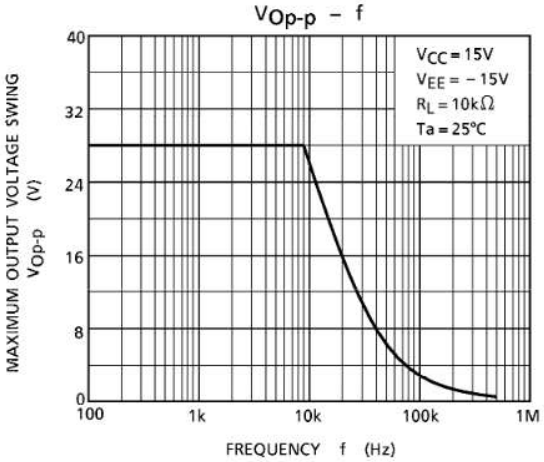
V_{Op-p} – R_L



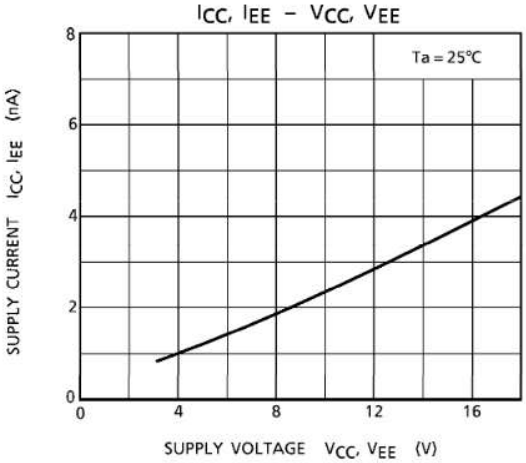
CMRR – f



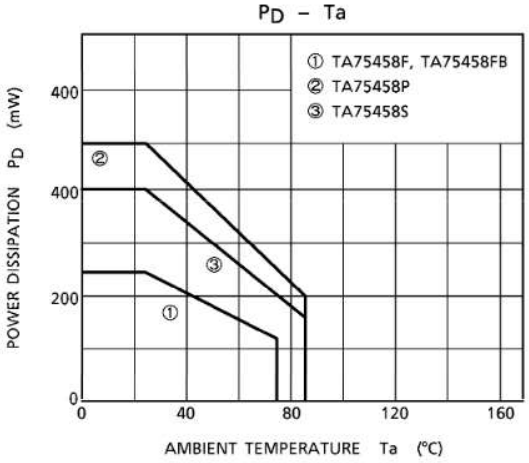
V_{Op-p} – f



I_{CC}, I_{EE} – V_{CC}, V_{EE}



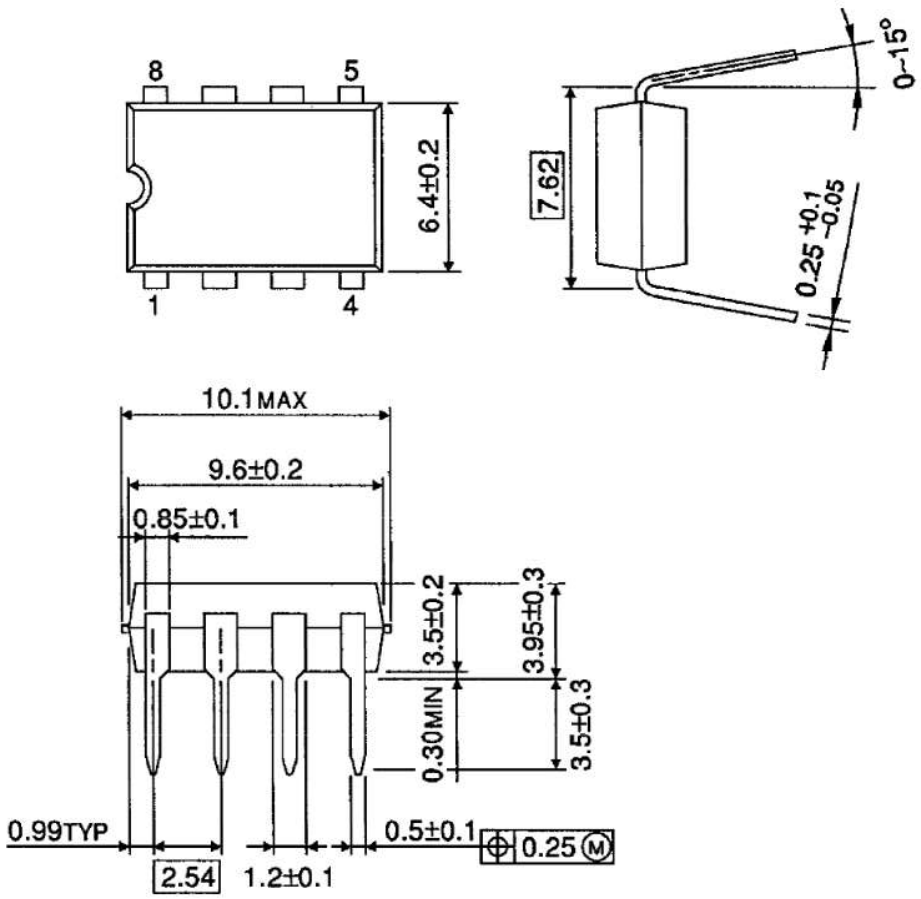
P_D – Ta



OUTLINE DRAWING

DIP8-P-300-2.54A

Unit : mm

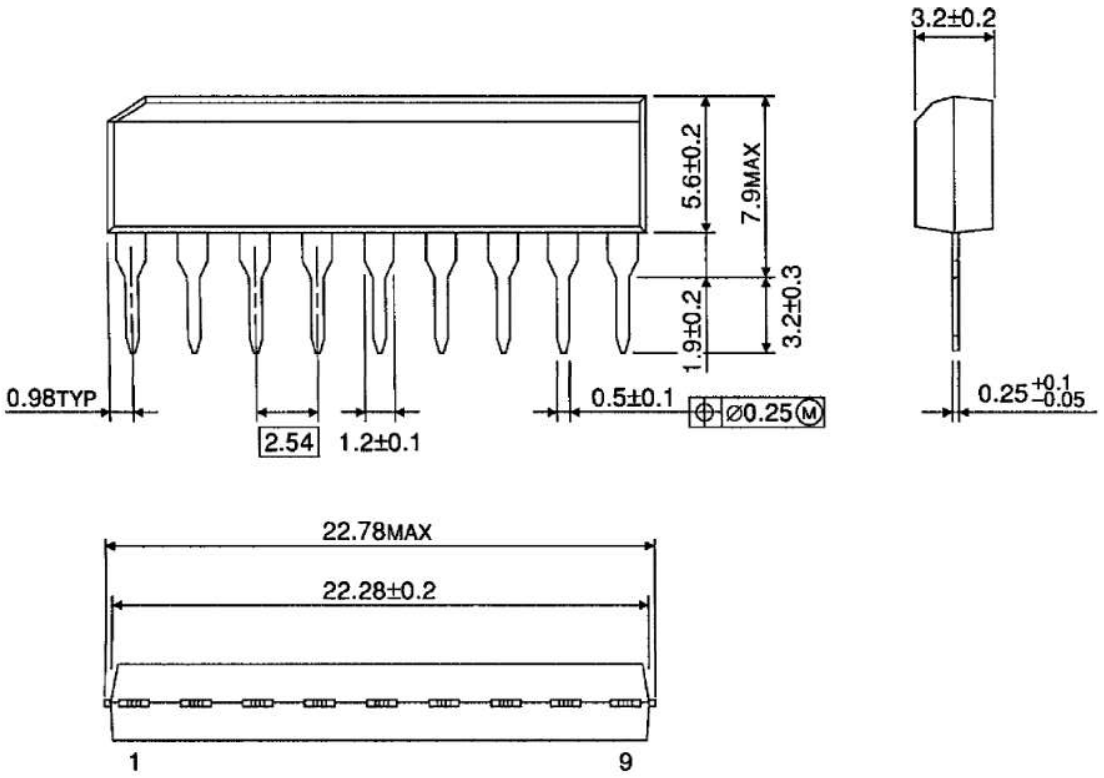


Weight : 0.5g (Typ.)

OUTLINE DRAWING

SIP9-P-2.54A

Unit : mm

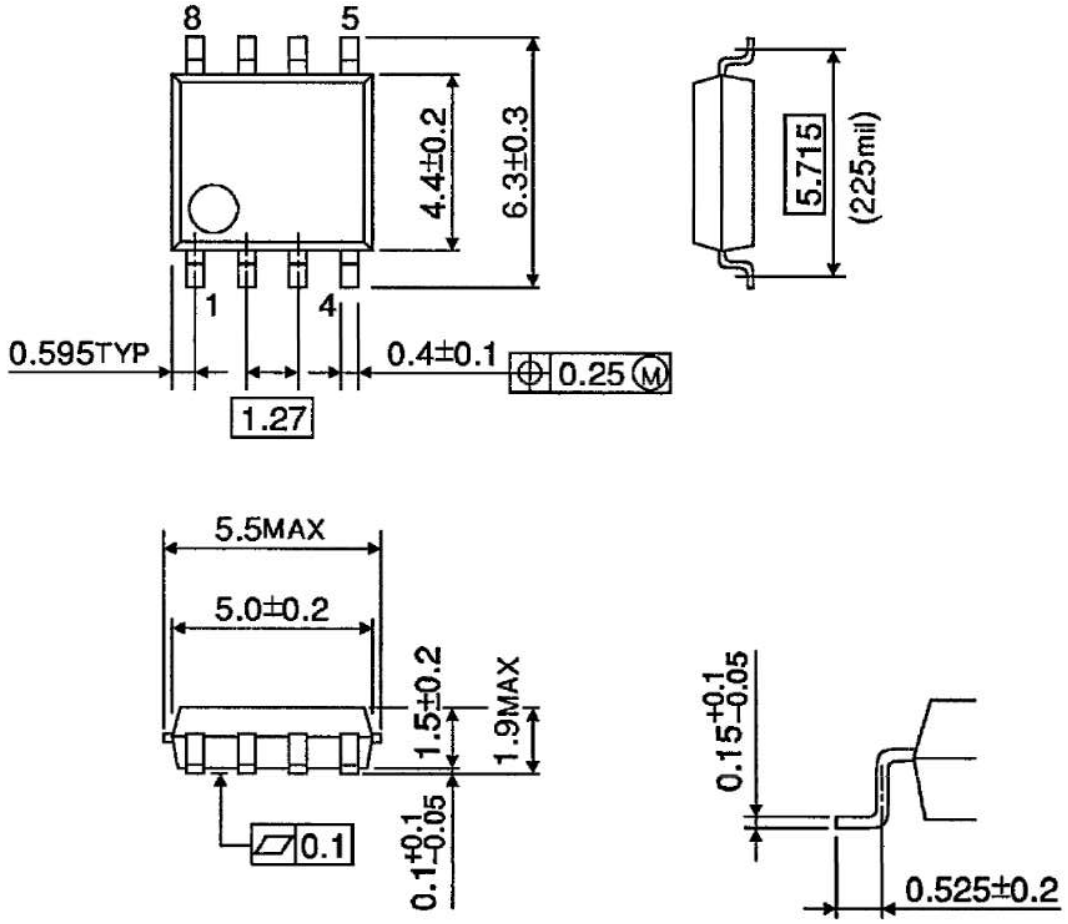


Weight : 0.9g (Typ.)

OUTLINE DRAWING

SOP8-P-225-1.27

Unit : mm

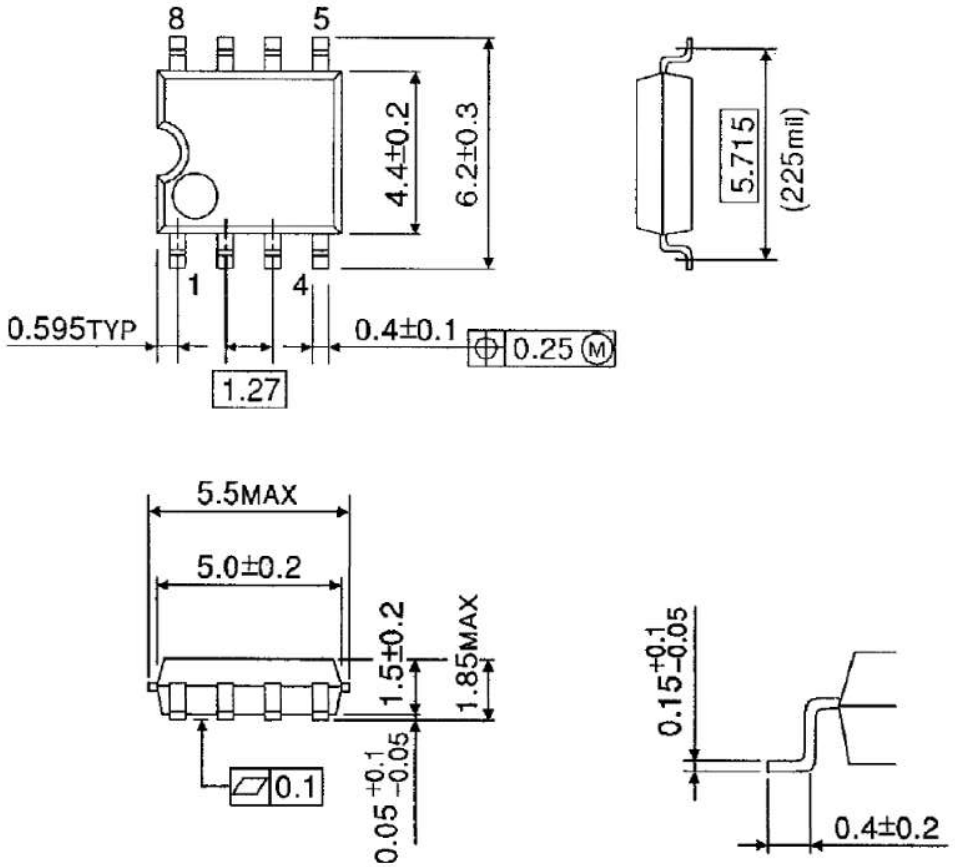


Weight : 0.1g (Typ.)

OUTLINE DRAWING

SOP8-P-225-1.27B

Unit : mm



Weight : 0.1g (Typ.)