

Quartz Clock Circuits Bipolar Stepper Motor Applications

FEATURES

- Single battery operation
- Very low current - typically 40 μ A at 4.19MHz
- Reset or stop function, inhibited during output
- Extremely low output saturation resistance: less than 100 ohms
- Complex direct drive alarm: 1Hz + 8Hz + 2048Hz
- Custom options available

ORDERING INFORMATION

DEVICE	MOTOR OUTPUT	ALARM OUTPUT
ICM7050	47ms @ 0.5 Hz	Complex
ICM1115	0.5 Hz Square Wave	64 Hz Tone

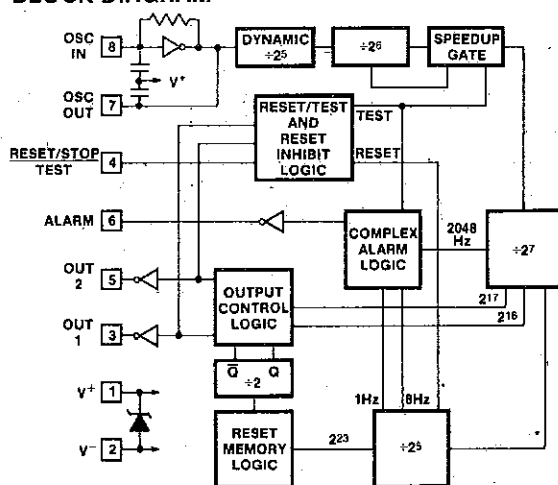
Note: These devices require a crystal frequency of 4.19 MHz.
Consult ICM7070 data sheet for 32.768 kHz devices.

*See PART NUMBER CHANGES below.

GENERAL DESCRIPTION

The ICM7050/ICM1115 are single battery analog quartz clock circuits intended for use with bipolar stepper motors and fabricated using Intersil's low voltage metal gate CMOS process. The circuits consist of a divider chain, output gating, output buffers and an oscillator which, when using the specified 4.19MHz crystal and capacitors, provides excellent stability. The high frequency portion of the divider chain consists of dynamic dividers, while the remainder are static. The dynamic dividers feature low power consumption and operating voltage, but limit low frequency operation. The 2²³ divider chain is tapped at the 2¹¹, 2¹⁹, and 2²² points to provide a complex alarm of 1Hz, 8Hz, and 2048Hz driving an output inverter. Several standard motor drive waveforms are available, and the large output inverters provide the low impedance necessary to drive the motor. A reset inhibit function is provided so that if the RESET occurs during an output pulse, resetting will not take place until the pulse is completed. RESET may also be used as a stop for synchronization to a time signal or tester. Motor drive will continue 1 sec. after RESET is released.

BLOCK DIAGRAM



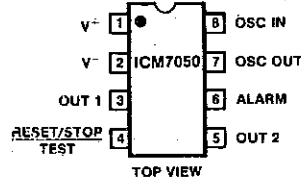
CUSTOM OPTIONS

The ICM7050 input and output configurations may be customized for:

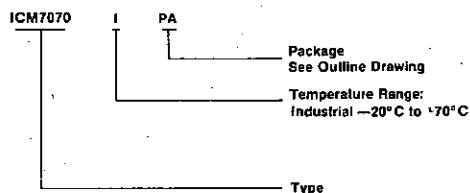
- On-chip oscillator capacitance up to 20 pF at OSC IN or OSC OUT
- Output pulse frequency from 0.5 Hz to 64 Hz (standard crystal freq.)
- Output pulse width from 0.98 msec to 50% duty cycle
- Alarm output up to three binary frequencies from 1 Hz to 2048 Hz

Consult factory for mask programming charge and minimum order requirements.

PIN CONFIGURATION (outline dwg PA)



ORDERING INFORMATION



Order Devices by Following Part Number — ICM7050IPA
ICM1115AIPA
ICM1115BIPA

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1)	300mW
Supply Voltage	3V
Output Voltage (Note 2)	Equal to but never
Input Voltage (Note 2)	exceeding the supply voltage
Storage Temperature	-30°C to +125°C
Operating Temperature	-20°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

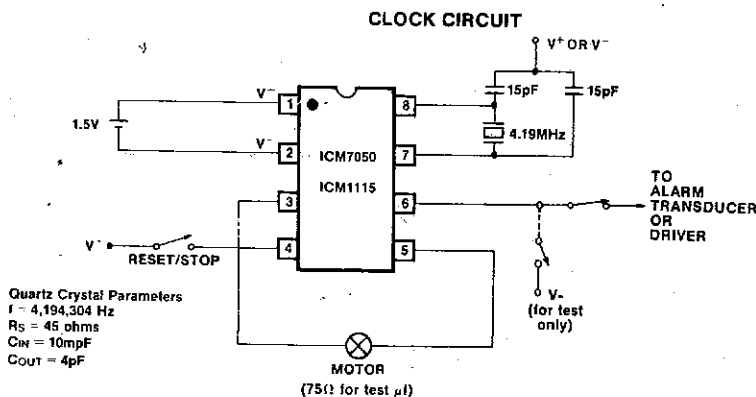
ELECTRICAL CHARACTERISTICS

($V^+ = 1.5V$, $f_{osc} = 4,194,304Hz$ test circuit, $T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 3) except ICM1115A	I^+	No Load		40	60	μA
ICM1115A Only				80	120	
Operating Voltage	V^+	$-20^\circ C < T_A < 70^\circ C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	$I_L = 4mA$		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, $I_L = 1mA$		400	700	Ω
		N, $I_L = 2mA$		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \leq V^+ \leq 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec
Oscillator Transconductance (Note 3)	g_m	ICM7050	75	200		
		ICM1115A	150	400		μmho
		ICM1115B	75	200		

NOTE 3: Two options are available with the ICM1115. The ICM1115B is designed to be used with crystals whose load capacitance is 12 pF or less. Using input and output capacitors of 15 to 20 pF, this device will provide stable operation at very low supply current. For applications with larger load capacitance (15 to 20 pF), the ICM1115A ensures that an increased oscillator current is available to guarantee startup and operation over the voltage range. Using input and output capacitors of 30 to 40 pF, the ICM1115A will offer good stability at a supply current approximately twice that of the ICM1115B.

TYPICAL APPLICATION (also TEST CIRCUIT)



Notes:

RESET/STOP: If pin 4 is not used, it should be tied to V^- .

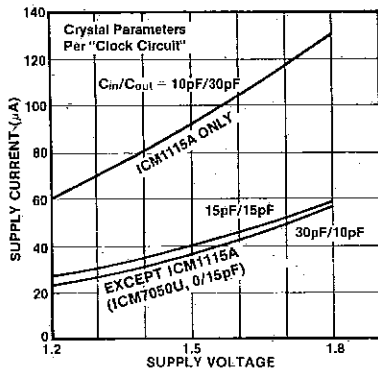
OUTPUT FREQUENCIES: Crystal frequencies from 1 to 10 MHz may be used to obtain different output frequencies. See Oscillator Considerations for suitable crystal parameters.

ICM7050/ICM1115

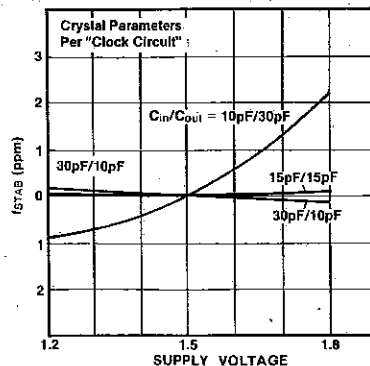


TYPICAL OPERATION CHARACTERISTICS

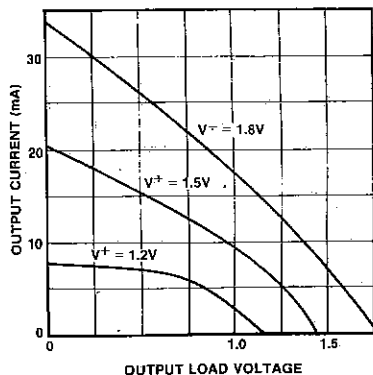
SUPPLY CURRENT vs SUPPLY VOLTAGE



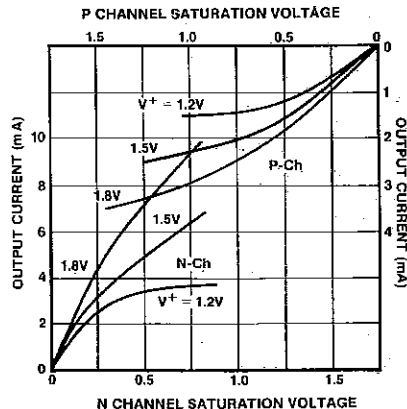
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



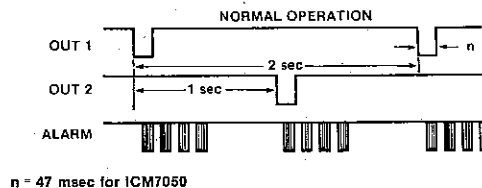
OUTPUT CURRENT vs OUTPUT LOAD VOLTAGE



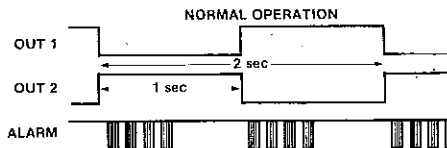
ALARM OUTPUT CURRENT vs SATURATION VOLTAGE



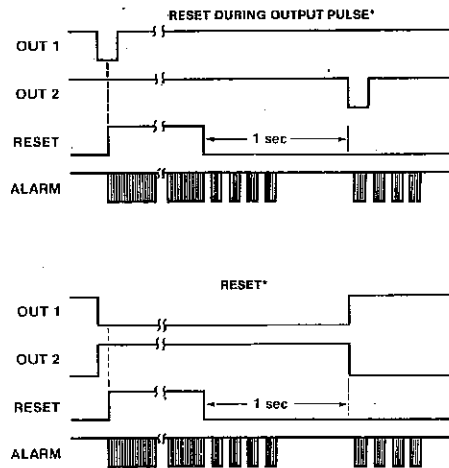
OUTPUT WAVEFORMS (ICM7050)



OUTPUT WAVEFORMS (ICM1115)



*Shown during Output 1; exchange Output 1 and Output 2 for opposite case.



APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7050 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15/15pF or 20/20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip. Oscillator tuning should be done at the OSCillator OUTput.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \quad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

g_m required for startup

$$g_m = \omega^2 C_{in}C_{out}R_s \left(1 + \frac{C_o}{C_L}\right)^2$$

R_s = series resistance of the crystal

f = frequency of the crystal

Δf = frequency shift from series resonance frequency

C_o = static capacitance of the crystal

C_{in} = input capacitance

C_{out} = output capacitance

C_m = motional capacitance

$\omega = 2\pi f$

The resulting g_m should not exceed 50 μ mhos.

OSCILLATOR TUNING METHODS

When tuning the oscillator two methods can be used. The first method would be to monitor the output pulse at either OUT 1 or OUT2 with a counter set to measure the period. The oscillator trimmer would then be adjusted for a reading of 2.000000 secs. A second method would be to put the device in the **reset** mode by pulling the RESET pin to V_+ and then monitor the ALARM output with a counter set to measure average period. The ALARM output is a continuous 2048Hz when in the **reset** mode, which gives a period of 488.28125 μ s.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

TEST MODE OPERATION

Pulling the RESET/TEST input to $-7V$ switches the device into the **test** mode to speedup automatic testing. When in the **test** mode the output rate is increased 16 times, from 1Hz to 16Hz, with a corresponding reduction in pulse width. The ALARM output changes to a composite waveform of 16Hz and 128Hz. The circuit can be **reset** while in the **test** mode by shorting the ALARM output to V_+ .

ALARM CONSIDERATIONS

The ALARM output inverter is large enough to directly drive transducers requiring up to 2mA of current. If more current is needed, a PNP buffer should be used*. A slight fluctuation in the supply current of 0.5 μ A to 1.0 μ A will be seen; this is a result of 2048Hz driving the relatively large gate capacitance of the alarm output transistors.

*See Intersil Application Bulletin A031 for details.

CHIP TOPOGRAPHY

