HD614P080S/ HD614P0160S

Description

The HD614P080S is a 4-bit single-chip microcomputer which can mount a standard EPROM 27128 for program memory. The HD614P0160S can mount a standard EPROM 27256.

The HD614P080S and HD614P0160S are pin-compatible with mask ROM HMCS402/404/408, but have some differences. By modifying the program in the EPROM, they can be used for the evaluation of the HMCS402/404/408 or for small-scale production.

Features

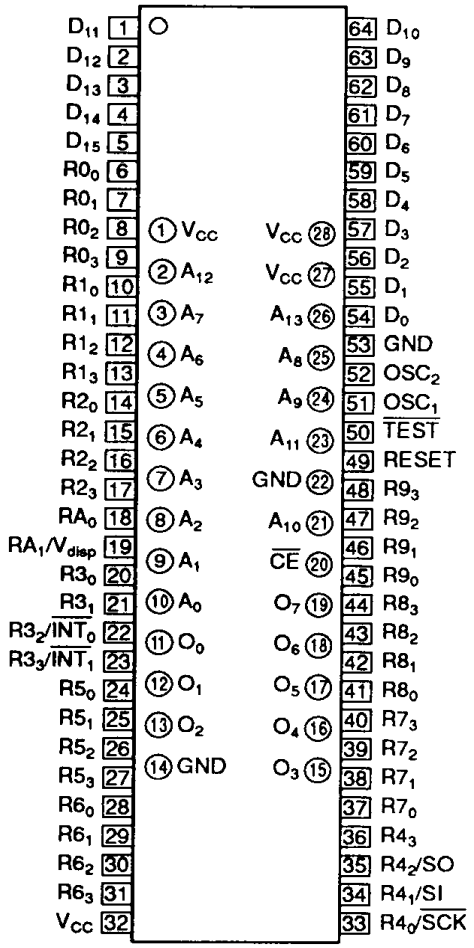
- Application for 4, 8, or 16 Kwords × 10 bits of EPROM
  - — 8192-word × 10-bit (HN27178A)
  - — 16384-word × 10-bit (HN27256)
- 576-digit × 4-bit RAM
- 58 I/O pins
  - — 26 high-voltage pins (up to 40 V max.)
  - — 32 standard pins
- Two timer/counters
  - — 11-bit prescaler
  - — 8-bit free-running timer
  - — 8-bit auto-reload timer/event counter
- Clock-synchronous 8-bit serial interface
- Five interrupt sources
  - — Two by external sources
  - — Two by timer/counters
  - — One by serial interface
- Subroutine stack up to 16 levels, including interrupts
- Minimum instruction execution time: 1.33 µs
- Two low power modes
  - — Standby: Stops instruction execution while keeping the clock generator, interrupt functions, timer/counters, and serial interface in operation
  - — Stop: Stops instruction execution and clock generation while retaining RAM data
- On-chip oscillator
  - — Crystal resonator or ceramic filter resonator (also externally drivable)
- Power voltage range: 5 V ±10%
- I/O pin circuit types:
  - — All standard pins are without pull-up MOS
  - — All high voltage pins are without pull-down MOS
- 64-pin shrink-type EPROM on-package

Recommended EPROMs

Type	Program Memory Capacity	f_{OSC} (MHz)	EPROM Type No.
HD614P080S	8192 words	6	HN27128A series
HD614P0160S	16384 words	4	HN27256 series
		6	HN27C256 series HN27C256A series HN27C256H series

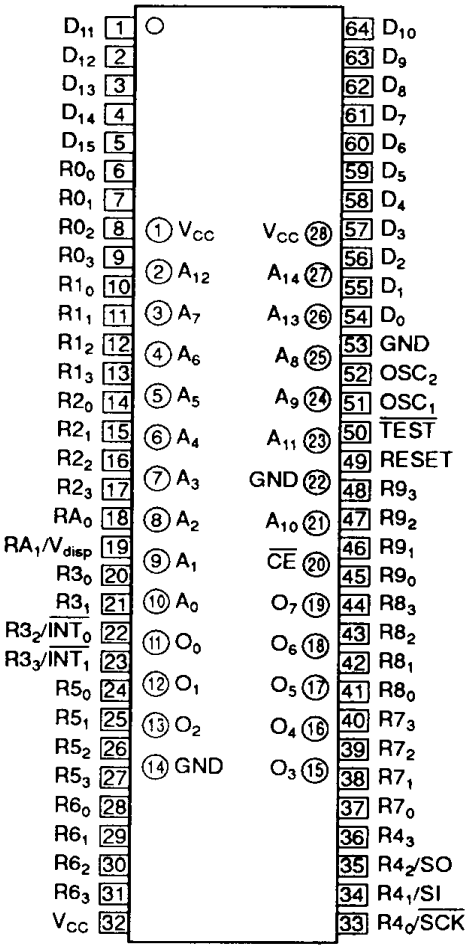
Pin Arrangement

HD614P080S



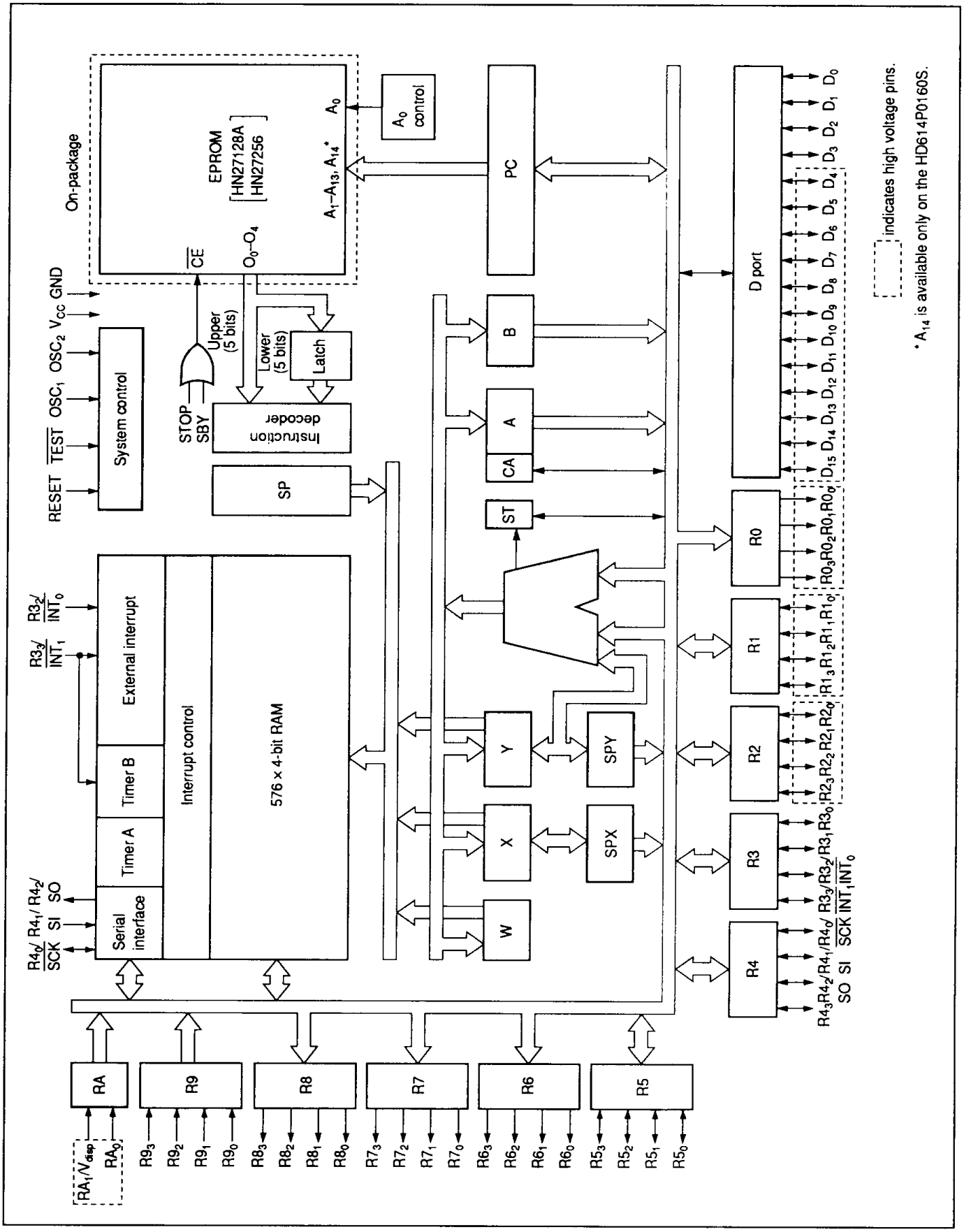
(Top view)

HD614P0160S



(Top view)

Block Diagram



Memory Map

ROM Memory Map

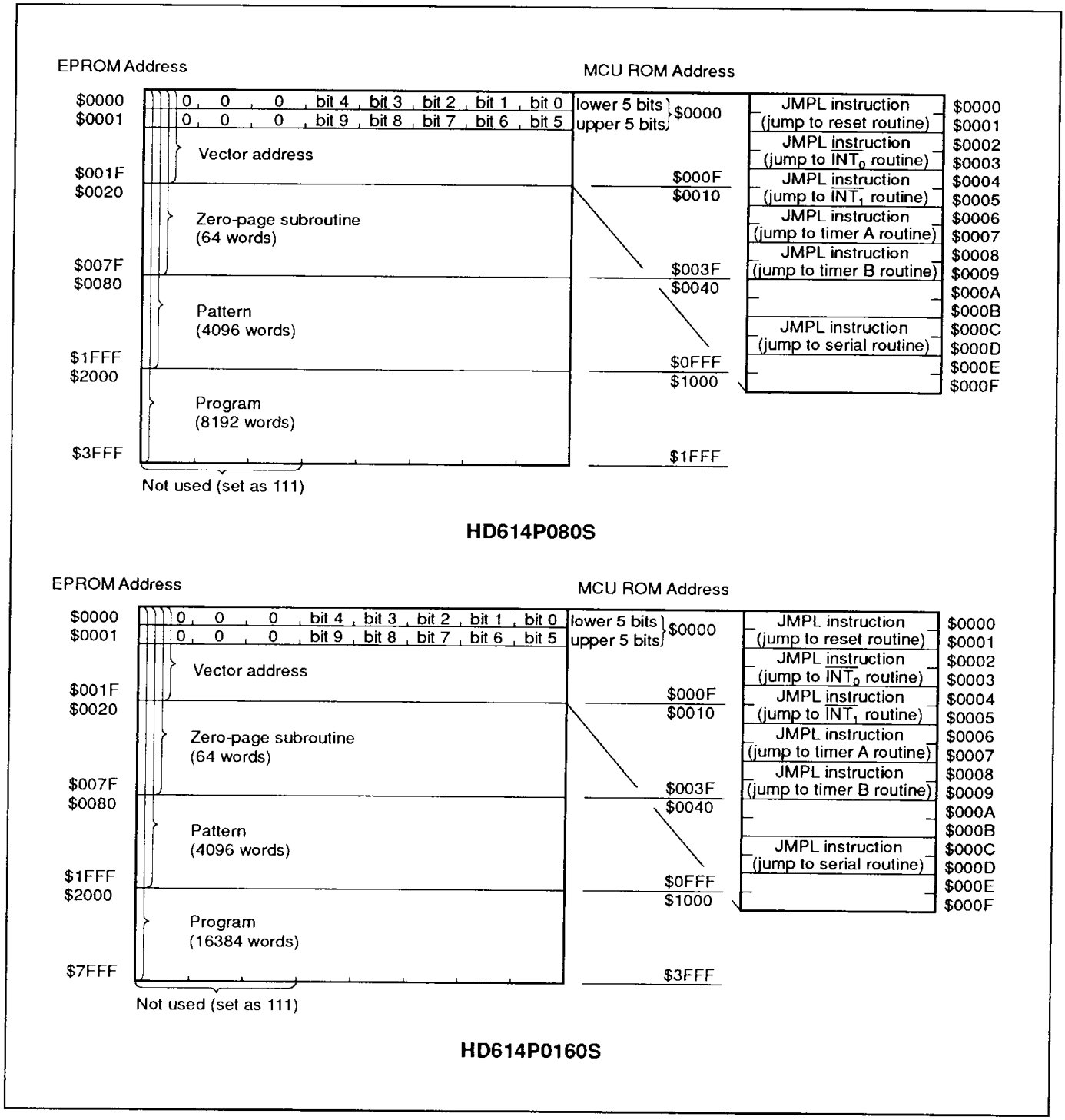


Figure 1 ROM Memory Map

RAM Memory Map

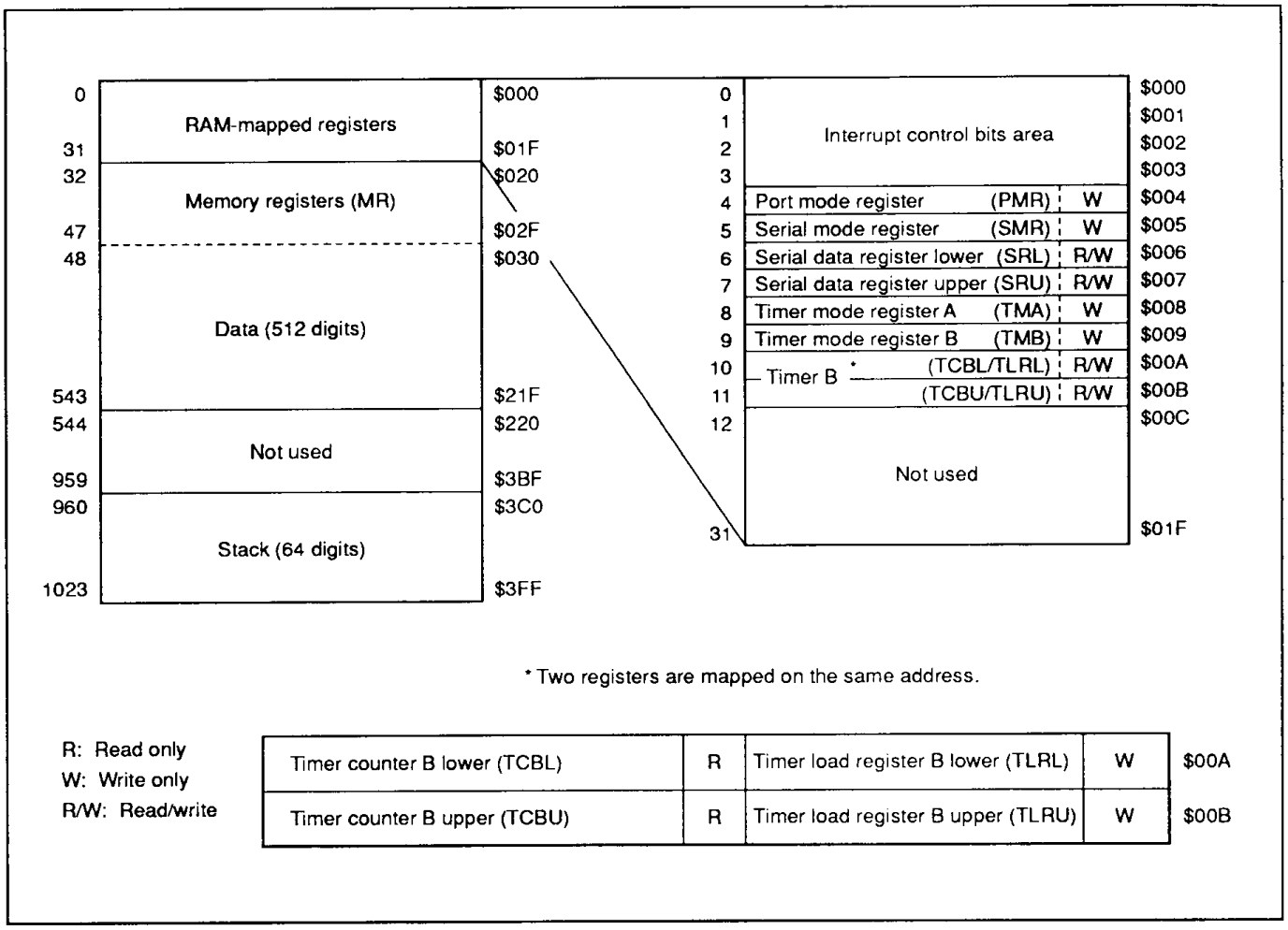


Figure 2 RAM Memory Map

Internal Oscillator Circuit

Figure 3 shows the block diagram of the internal oscillator circuit. The oscillator type can be selected as a crystal resonator or ceramic filter resonator as shown in table 1. In any case, an external clock operation is available.

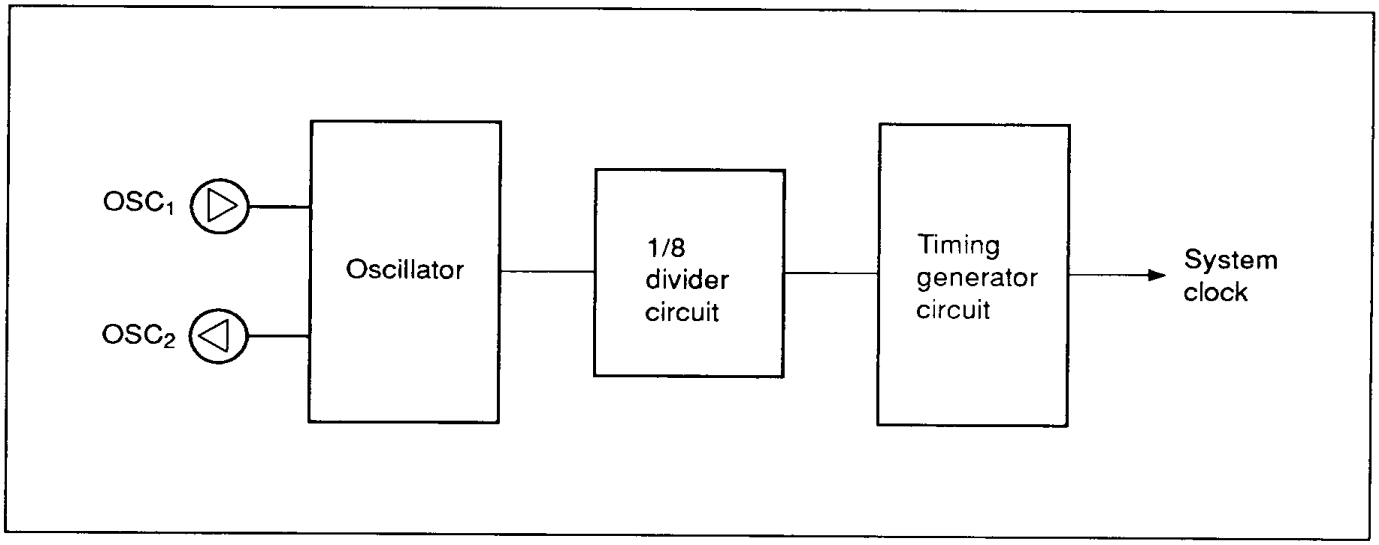


Figure 3 Internal Oscillator Circuit

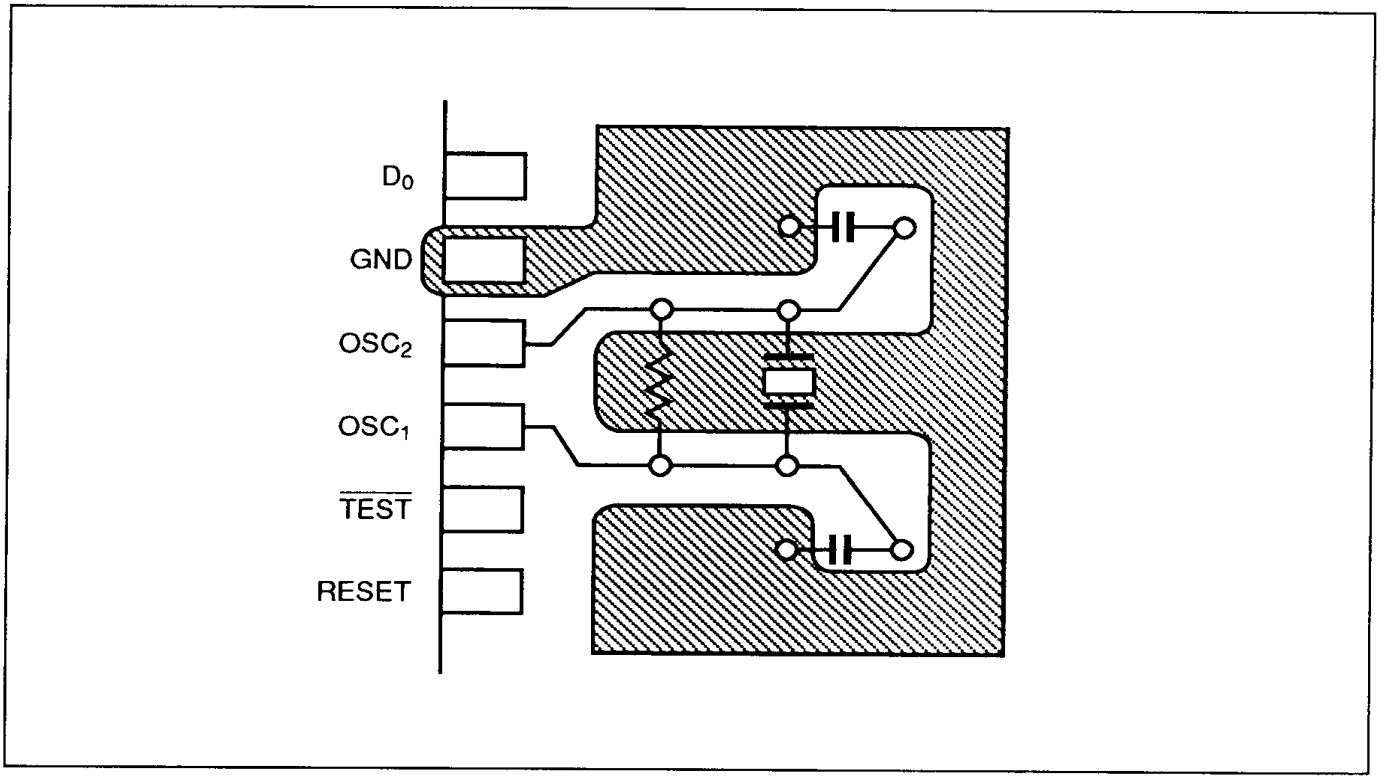
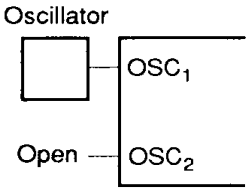
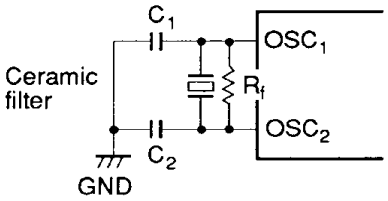
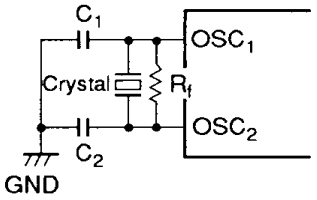
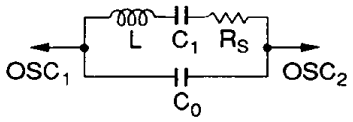


Figure 4 Layout of Crystal and Ceramic Filter

Table 1 Oscillator Circuit Examples

	Circuit Configuration	Remarks
External clock operation		
Ceramic filter resonator		Ceramic filter: CSA 4.00MG (Murata) R_f: 1 MΩ ±2% C_1: 33 pF ±20% C_2: 33 pF ±20% Ceramic filter: CSA 6.00MG (Murata) R_f: 1 MΩ ±2% C_1: 30 pF ±20% C_2: 30 pF ±20%
Crystal resonator	 AT-cut parallel resonance crystal 	Crystal: 4.194304 (MHz) NC-18C (Nihon Denpa Kogyo) R_f: 1 MΩ ±2% C_1: 22 pF ±20% C_2: 22 pF ±20% Crystal: 6.0 (MHz) NC-18C (Nihon Denpa Kogyo) R_f: 1 MΩ ±2% C_1: 20 pF ±20% C_2: 20 pF ±20% Crystal: AT-cut parallel resonance crystal C_o: 7 pF max. R_s: 100 Ω max. f: 2.0–6.2 MHz

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic filter maker. The circuit parameters are affected by the crystal, ceramic filter resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic filter maker to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic filter.

Input/Output

The MCU provides 58 I/O pins, consisting of 32 standard pins of without pull-up MOS (NMOS open drain) and 26 high voltage pins of without pull-down MOS (PMOS open drain).

When any common input/output pin is used as input, it becomes necessary to set the output data as shown in table 3.

Table 2 I/O Pin Circuit Types

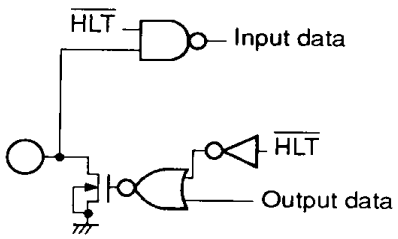
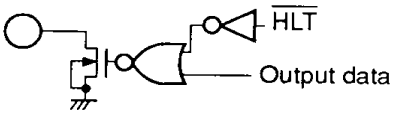
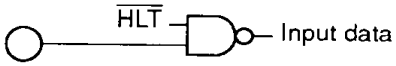
		Without Pull-Up MOS (NMOS Open Drain)	Applied Pins
Standard pins	Common I/O pins		D_0–D_3, $R3_0$–$R3_3$, $R4_0$–$R4_3$, $R5_0$–$R5_3$
	Output pins		$R6_0$–$R6_3$, $R7_0$–$R7_3$, $R8_0$–$R8_3$
	Input pins		$R9_0$–$R9_3$

Table 2 I/O Pin Circuit Types (cont)

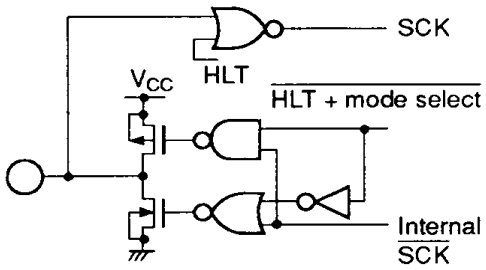
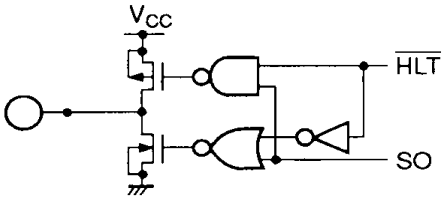
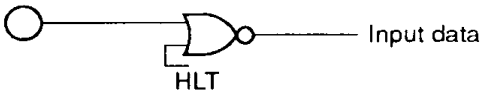
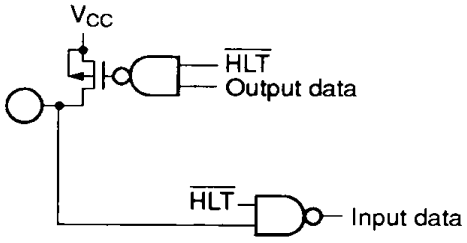
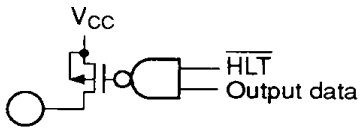
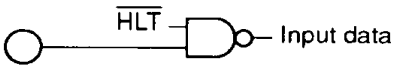
		Without Pull-Up MOS (NMOS Open Drain)	Applied Pins
Standard pins (cont)	Common I/O pins		$\overline{SCK}$ (Note 2) (Output Mode)
	Output pins		SO
	Input pins		$\overline{INT_0}$, $\overline{INT_1}$, SI, $\overline{SCK}$ (Note 2) (Input Mode)

Table 2 I/O Pin Circuit Types (cont)

		Without Pull-Down MOS (PMOS Open Drain)	Applied Pins
High voltage pins	Common I/O pins		D_4–D_{15}, $R1_0$–$R1_3$, $R2_0$–$R2_3$
	Output pins		$R0_0$–$R0_3$
	Input pins		RA_0, RA_1/V_{disp}

Notes: 1. In the stop mode, $\overline{HLT}$ is 0, HLT is 1, and I/O pins are in high impedance.
2. If the MCU is interrupted by the serial interface in the external clock input mode, the $\overline{SCK}$ terminal becomes input only.

Table 3 Data Input from Common Input/Output Pins

I/O Circuit Type	Available Pin Condition for Input
For standard pins of without pull-up MOS (NMOS open drain)	1
For high voltage pins of without pull-down MOS (PMOS open drain)	0

Differences Between In-Package PROM, On-Package EPROM, and Mask ROM Types

Item		In-Package PROM ZTAT™ HD4074019				In-Package PROM ZTAT™ HD4074008			On-Package EPROM HD614P080S HD614P0160S	Mask ROM HD404019		Mask ROM HMCS408AC/C/CL			Mask ROM HMCS404AC/C/CL			Mask ROM HMCS402AC/C/CL	
Typical instruction execution time		1 µs				1 µs			1.33 µs	1 µs		1 µs	2 µs	4 µs	1 µs	2 µs	4 µs	1 µs	2 µs	4 µs
Power supply voltage (V)		4.5–5.5				4.5–5.5			4.5–5.5	3.5–6		4.5–6	3.5–6	2.5–6	4.5–6	4–6	2.7–6	4.5–6	4–6	2.7–6
ROM		16,384 words x 10-bit				8,192 words x 10-bit			HN27C64: 4,096 x 10-bit HN4827128: 8,192 x 10-bit HN27C256: 16,384 x 10-bit	16,384 words x 10-bit		8,192 words x 10-bit			4,096 words x 10-bit			2,048 words x 10-bit	
RAM		992 x 4-bit				512 x 4-bit			576 x 4-bit	992 x 4-bit		512 x 4-bit			256 x 4-bit			160 x 4-bit	
I/O pin	Standard circuit	NMOS open drain pins				NMOS open drain			NMOS open drain	Each pin can be without pull-up MOS (NMOS open drain), with pull-up MOS, or CMOS									
	High voltage pins	PMOS open drain				PMOS open drain (Typical 5-V use)			PMOS open drain	Each pin can be without pull-down MOS (PMOS open drain) or with pull-down MOS									
Clock generation	Crystal	o				o			o	o		o			o			o	
	Ceramic	o				o			o	o		o			o			o	
	Resistance	—				—			—	—		—			HMCS404C			HMCS402C	
Package	Type	DC-64S (Window)	DP-64S	FP-64B	FP-64A	DC-64S (Window)	DP-64S	FP-64 FP-64A	DC-64SP	DP-64S	FP-64B	FP-64A	DP-64S	FP-64	DP-64S	FP-64		DP-64S	FP-64
	Occupied area (mm)	18.8 x 57.3	17 x 58	18.8 x 24.8	17.2 x 17.2	18.8 x 57.3	17 x 58	19.6 x 25.6 17.2 x 17.2	23 x 57.3	17 x 58	18.8 x 24.8	17.2 x 17.2	17 x 58	19.6 x 25.6	17 x 58	19.6 x 25.6		17 x 58	19.6 x 25.6
	Height from stand off (mm)	5.6 (Max)	5.1 (Max)	2.9 (Max)	2.9 (Max)	5.6 (Max)	5.1 (Max)	2.9 (Max) 2.9 (Max)	7.5 (Max)	5.1 (Max)	2.9 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)		5.1 (Max)	2.9 (Max)

Notes: DC-64S: 64-pin shrink type ceramic DIP with window
DP-64S: 64-pin shrink type DIP
FP-64: 64-pin flat plastic package
DC-64SP: 64-pin shrink type ceramic EPROM on-package
o: Available
—: Not available

Precautions When Using the EPROM On-Package Microcomputer

Pay careful attention to the following since this MCU is particularly structured with pin sockets on its package.

1. Avoid contact of high static or surge voltages so as to not exceed the maximum ratings of the socket pins as well as the LSI pins. If such a contact is made, the device may become permanently damaged.

2. When using this chip in production (i.e., for mask ROM single chip microcomputers), pay special attention to the following to maintain a solid connection between the EPROM pins and the socket pins.

   a. The recommended conditions for soldering the chip onto a circuit board are:

      Temperature: Below 250°C
      Time: Within 10 seconds

      If these conditions are exceeded, the bonding solder of the solder pins may melt, thus causing the solder pins to move about.

   b. Avoid getting any detergent or coating inside the sockets during flux washing or board coating after soldering. Doing so may cause poor contact within the sockets.

   c. Avoid permanent use of this chip in a vibratory environment or system.

   d. The sockets lose contact after being used repeatedly so it is recommended to use a new chip during production.

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	−0.3 to +7.0	V	
Pin voltage	V_T	−0.3 to V_{CC} + 0.3	V	3
		V_{CC} − 45 to V_{CC} + 0.3	V	4
Total permissible input current	ΣI_o	50	mA	5
Total permissible output current	$-\Sigma I_o$	150	mA	6
Maximum input current	I_o	15	mA	7, 8
Maximum output current	$-I_o$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes: 1. Permanent damage may occur if these absolute maximum ratings of the LSI or the EPROM are exceeded. Normal operation should be under the conditions of the electrical characteristics. If these conditions are exceeded, it may cause a malfunction and affect the reliability of the LSI.
2. All voltages are with respect to GND.
3. Applied to standard pins.
4. Applied to high voltage I/O pins.
5. Total permissible input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
6. Total permissible output current is the total sum of the outputs currents which flow out from V_{CC} to all I/O pins simultaneously.
7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
8. Applied to D_0–D_3 and R3–R8.
9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
10. Applied to D_0–D_3 and R3–R8.
11. Applied to R0–R2.
12. Applied to D_4–D_{15}.

Electrical Characteristics

DC Characteristics (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, if not specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	0.7V_{CC}	—	V_{CC} + 0.3	V		
		SI	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$	–0.3	—	0.22V_{CC}	V		
		SI	–0.3	—	0.22V_{CC}	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
			V_{CC} – 0.3	—	—	V	$-I_{OH}$ = 0.01 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO	—	—	0.4	V	I_{OL} = 1.6 mA	
Input/output leakage current	$\|I_{IL}\|$	RESET, SCK, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, OSC_1	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Current dissipation in mode	I_{CC}	V_{CC}	—	—	2.0	mA	V_{CC} = 5 V Crystal or ceramic filter resonator f_{OSC} = 4 MHz	2, 5
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.2	mA	Maximum logic operation V_{CC} = 5 V Crystal or ceramic filter resonator f_{OSC} = 4 MHz	3, 5
	I_{SBY2}	V_{CC}	—	—	0.9	mA	Minimum logic operation V_{CC} = 5 V Crystal or ceramic filter resonator f_{OSC} = 4 MHz	4, 5
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} to V_{CC} – 0.3 V $V_{in\ (RESET)}$ = 0 to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2.0	—	—	V		

Notes: 1. Output buffer current is excluded.

2. The MCU is in the reset state. The input/output current does not flow.

   Test conditions: MCU state
   - Reset state in operation mode

   Pin state
   - RESET, $\overline{TEST}$: V_{CC}
   - D_0–D_3, R3–R9: V_{CC}
   - D_4–D_{15}, R0–R2, RA_0, RA_1: V_{CC} to V_{CC} – 40 V

3. The timer/counter operates with the fastest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2 prescaler divide ratio
   - Timer B: Divide-by-2 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0–D_3, R3–R9: V_{CC}
   - D_4–D_{15}, R0–R2, RA_0, RA_1: V_{CC} to V_{CC} – 40 V

4. The timer/counter operates with the slowest clock and input/output current does not flow.

   Test conditions: MCU state
   - Standby mode
   - Input/output: Reset state
   - Timer A: Divide-by-2048 prescaler divide ratio
   - Timer B: Divide-by-2048 prescaler divide ratio
   - Serial interface: Stop

   Pin state
   - RESET: GND
   - $\overline{TEST}$: V_{CC}
   - D_0–D_3, R3–R9: V_{CC}
   - D_4–D_{15}, R0–R2, RA_0, RA_1: V_{CC} to V_{CC} – 40 V

5. The current consumption in the operation and standby modes is proportional to f_{OSC}. When $f_{OSC} = \chi$ [MHz], the current dissipation in operation mode and standby mode is estimated as follows:

$$\text{Max. value } (f_{OSC} = \chi) = \frac{\chi}{4} \times \text{max. value } (f_{OSC} = 4 \text{ MHz}).$$

Input/Output Characteristics for Standard Pins (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, if not specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	D_0–D_3, R3–R5, R9	$0.7V_{CC}$	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	D_0–D_3, R3–R5, R9	–0.3	—	$0.22V_{CC}$	V	
Output low voltage	V_{OL}	D_0–D_3, R3–R8	—	—	0.4	V	I_{OL} = 1.6 mA
Input/output leakage current*	$\|I_{IL}\|$	D_0–D_3, R3–R9	—	—	1	µA	V_{in} = 0 V to V_{CC}

* Output buffer current is excluded.

Input/Output Characteristics for High Voltage Pins (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, if not specified)

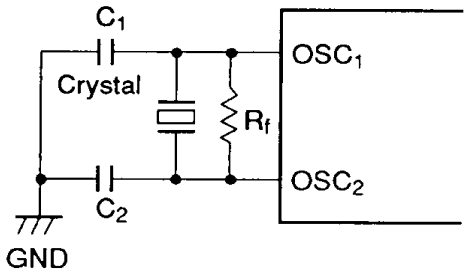
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	D_4–D_{15}, R1, R2, RA_0, RA_1	$0.7V_{CC}$	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	D_4–D_{15}, R1, R2, RA_0, RA_1	V_{CC} – 40	—	$0.22V_{CC}$	V	
Output high voltage	V_{OH}	D_4–D_{15}	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA
			V_{CC} – 2.0				$-I_{OH}$ = 9 mA
		R0–R2	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 3 mA
			V_{CC} – 2.0				$-I_{OH}$ = 1.8 mA
Output low voltage	V_{OL}	D_4–D_{15}, R0–R2	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V
Input/output leakage current*	$\|I_{IL}\|$	D_4–D_{15}, R0–R2, RA_0, RA_1	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}

* Output buffer current is excluded.

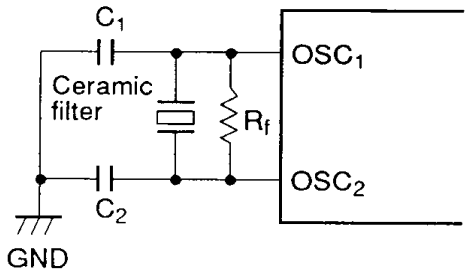
AC Characteristics (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, if not specified)

Item		Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Crystal resonator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	—	6.2	MHz		
	Instruction cycle time	t_{cyc}		1.29	—	20	µs		
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
Ceramic filter resonator	Oscillation frequency	f_{OSC}	OSC_1, OSC_2	0.4	—	6.2	MHz		
	Instruction cycle time	t_{cyc}		1.29	—	20	µs		
	Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	20	ms		1
External clock	External clock frequency	f_{CP}	OSC_1	0.4	—	6.2	MHz		2
	External clock high width	t_{CPH}	OSC_1	70	—	—	ns		2
	External clock low width	t_{CPL}	OSC_1	70	—	—	ns		2
	External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
	External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
	Instruction cycle time	t_{cyc}		1.29	—	20	µs		2
$\overline{INT_0}$ high width		t_{I0H}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_0}$ low width		t_{I0L}	$\overline{INT_0}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ high width		t_{I1H}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
$\overline{INT_1}$ low width		t_{I1L}	$\overline{INT_1}$	2	—	—	t_{cyc}		3
RESET high width		t_{RSTH}	RESET	2	—	—	t_{cyc}		4
Input capacitance		C_{in}	All pins	—	—	15	pF	f = 1 MHz V_{in} = 0 V	
Reset fall time		t_{RSTf}		—	—	20	ms		4

Notes: 1. The oscillator stabilization time is the period from when V_{CC} reaches its minimum allowable voltage V_{CC} = 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes high. At power-on or when recovering from stop mode, apply the RESET input for more than t_{RC} to meet the necessary time for oscillator stabilization. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, consult with the crystal or ceramic filter manufacturer when designing the reset circuit.

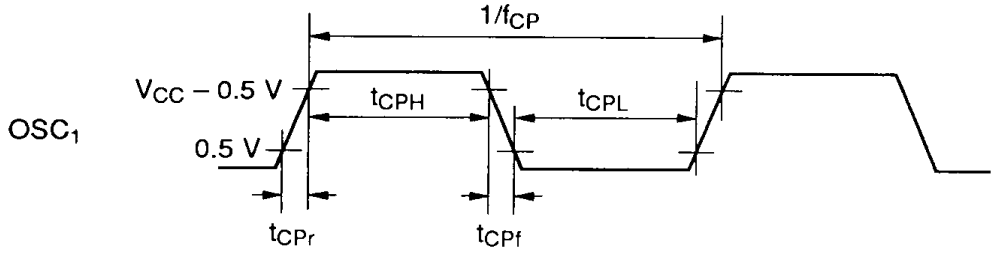


Crystal: 6.0 MHz
NC-18C (Nihon Denpa Kogyo)
R_f = 1 MΩ ±2%, C_1 = C_2 = 20 pF ±20%

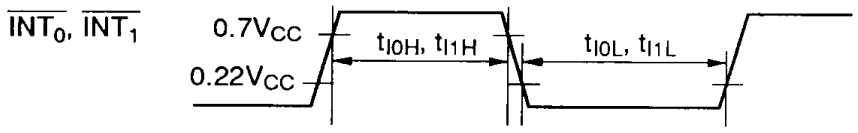


Ceramic filter: CSA6.00 MG (Murata)
R_f = 1 MΩ ±2%, C_1 = C_2 = 30 pF ±20%

2.



3.



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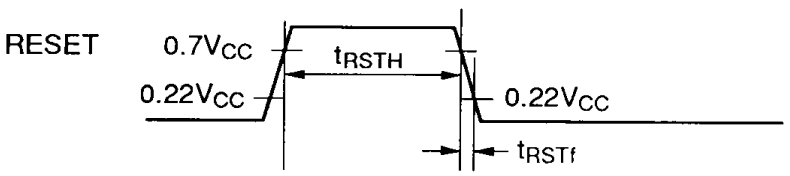


Serial Interface Timing Characteristics (V_{CC} = 4.5 V to 5.5 V, GND = 0 V, T_a = –20° to +75°C, if not specified)

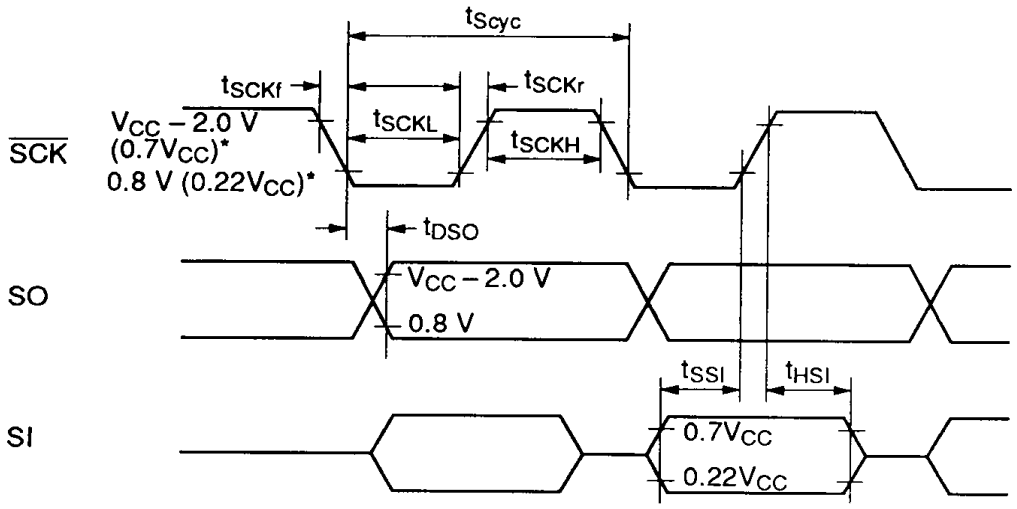
During Transmit Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}	See note 2	1, 2
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}	See note 2	1, 2
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns	See note 2	1, 2
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

During Transmit Clock Input

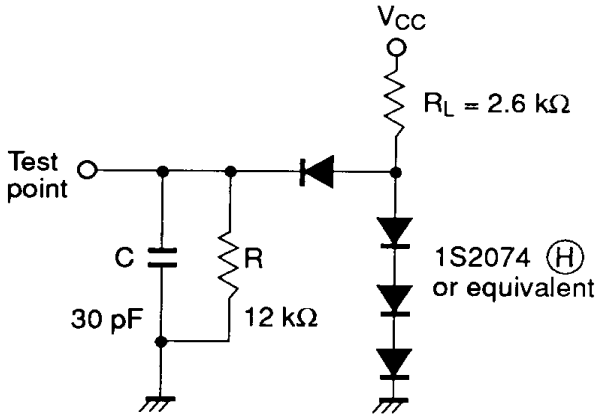
Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	t_{cyc}		1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	t_{Scyc}		1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	100	ns		1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	100	ns		1
Serial output data delay time	t_{DSO}	SO	—	—	250	ns	See note 2	1, 2
Serial input data setup time	t_{SSI}	SI	300	—	—	ns		1
Serial input data hold time	t_{HSI}	SI	150	—	—	ns		1

Notes: 1. Timing of serial interface

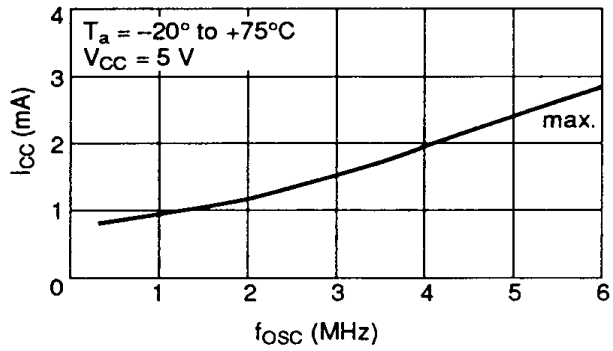


* V_{CC} – 2.0 V and 0.8 V are the threshold voltages for transmit clock output.
$0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltages for transmit clock input.

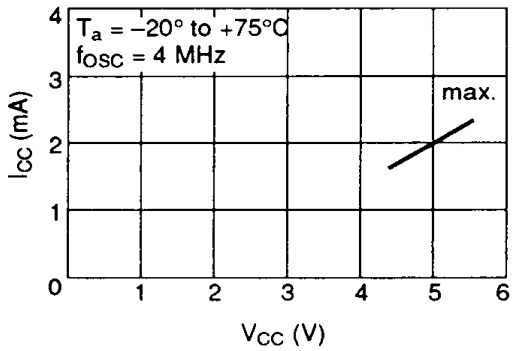
2. Timing load circuit



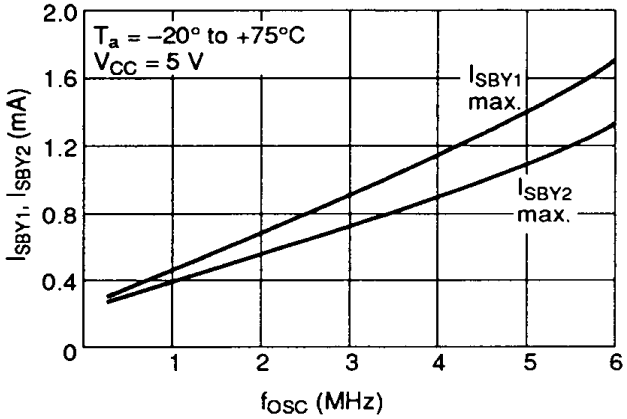
Characteristics Curves (Reference Data)



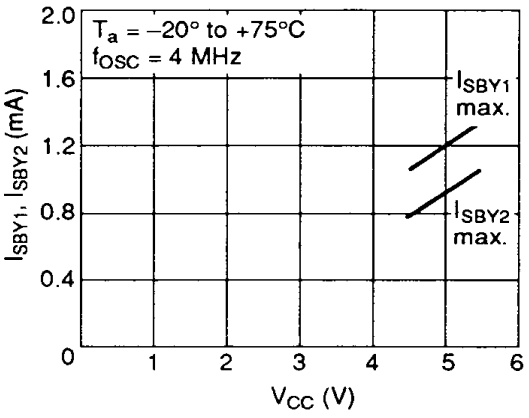
I_{CC} vs. f_{OSC} Characteristic
(Crystal, ceramic resonator)



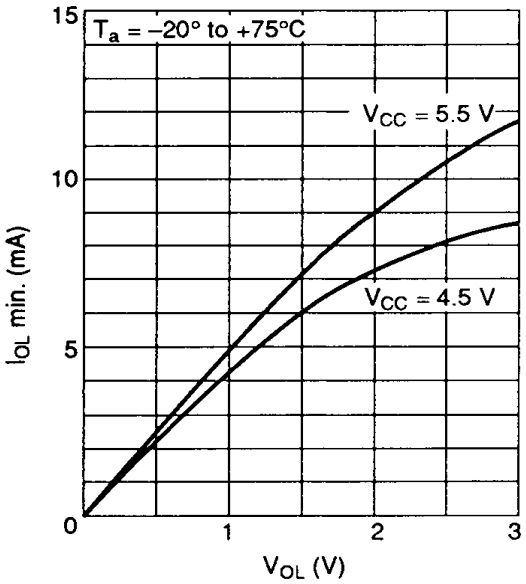
I_{CC} vs. V_{CC} Characteristic
(Crystal, ceramic resonator)



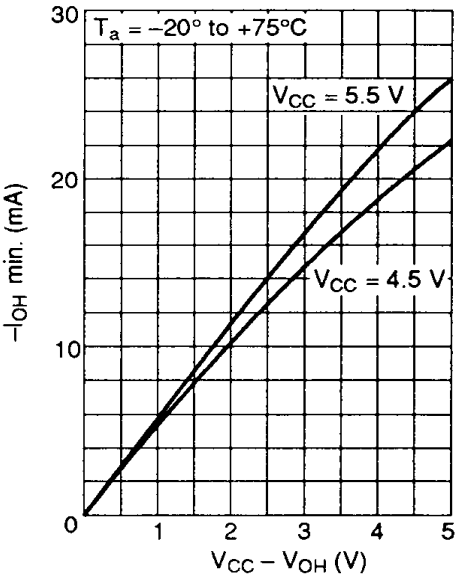
I_{SBY} vs. f_{OSC} Characteristic
(Crystal, ceramic resonator)



I_{SBY} vs. V_{CC} Characteristic
(Crystal, ceramic resonator)

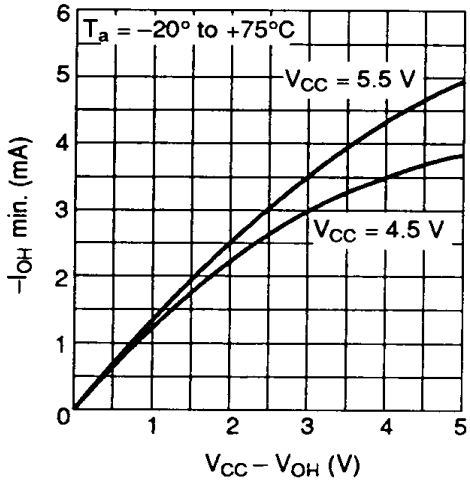


I_{OL} Minimum vs. V_{OL} Characteristic
(Standard pin)



$-I_{OH}$ Minimum vs. ($V_{CC} - V_{OH}$)
Characteristic (D_4–D_{15} pins)

Characteristics Curves (Reference Data) (cont)



$-I_{OH}$ Minimum vs. ($V_{CC} - V_{OH}$) Characteristic (R0–R2 pins)