

32K x 16 Static RAM

Features

- **High speed**
 - $t_{AA} = 12, 15 \text{ ns}$
- **CMOS for optimum speed/power**
- **Low active power**
 - 825 mW (max.)
- **Low CMOS standby power**
 - 16.5 mW (max.)
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in lead-free and non-lead-free 44-pin TSOP II and 44-pin (400-mil) SOJ packages**

Functional Description

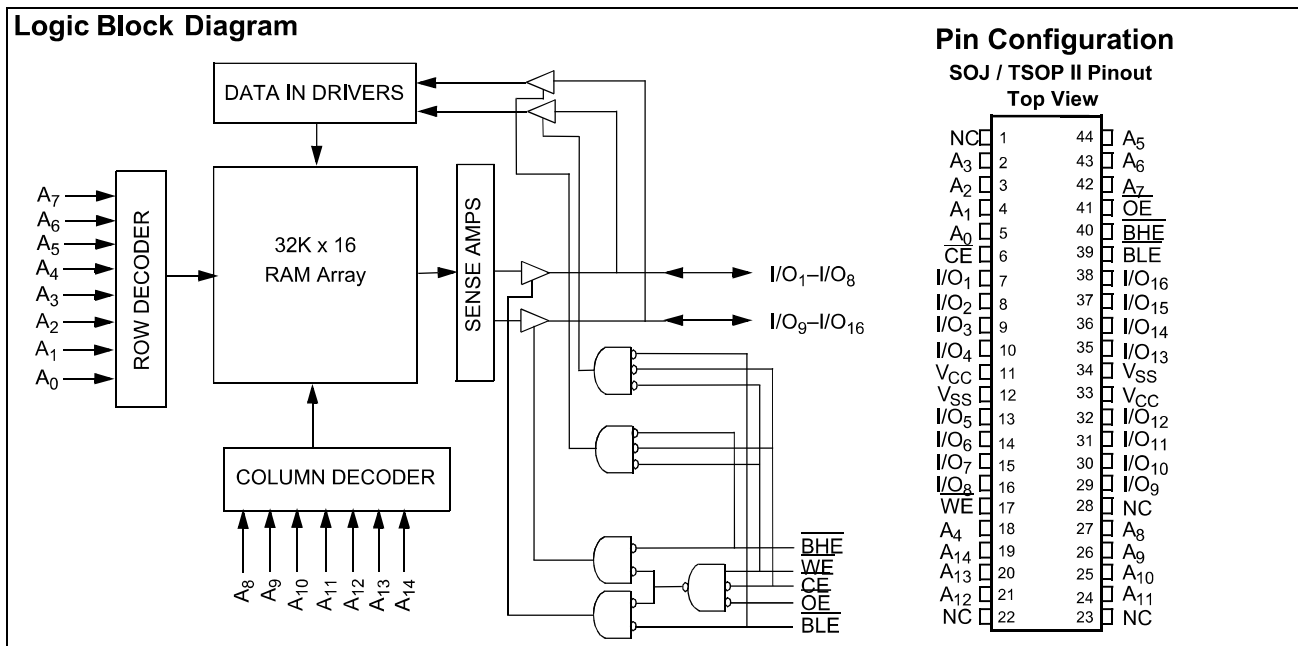
The CY7C1020B is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1020B is available in standard 44-pin TSOP Type II and 44-pin 400-mil-wide SOJ packages.



Selection Guide

	CY7C1020B-12	CY7C1020B-15
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	140	130
Maximum CMOS Standby Current (mA)	3	3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} Relative to GND^[1] -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY7C1020B-12		CY7C1020B-15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	μA
I_{OS}	Output Short Circuit Current ^[3]	$V_{CC} = \text{Max.}$, $V_{OUT} = GND$		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$		140		130	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		20		20	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$		3		3	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	pF

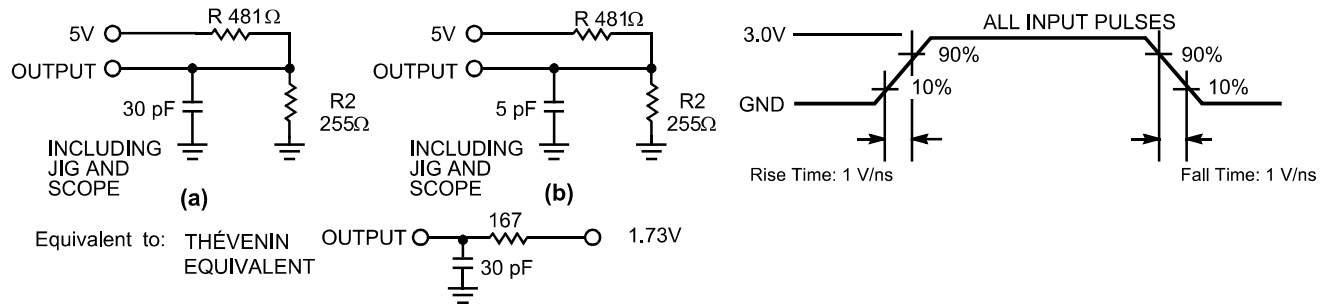
Thermal Resistance^[4]

Parameter	Description	Test Conditions	TSOP II Package	SOJ Package	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	50.55	56.31	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		15.8	32.9	°C/W

Notes:

- $V_{IL}(\text{min.}) = -2.0V$ for pulse durations of less than 20 ns.
- T_A is the case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics^[5] Over the Operating Range

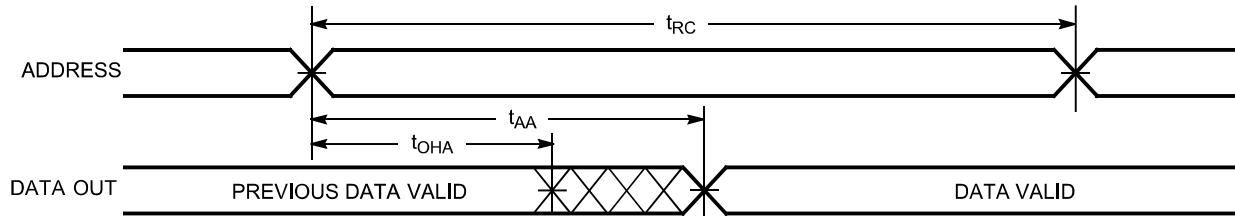
Parameter	Description	CY7C1020B-12		CY7C1020B-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	12		15		ns
t _{AA}	Address to Data Valid		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15	ns
t _{DOE}	\overline{OE} LOW to Data Valid		6		7	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[6]	0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		6		7	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		6		7	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15	ns
t _{DBE}	Byte Enable to Data Valid		6		7	ns
t _{LZBE}	Byte Enable to Low Z	0		0		ns
t _{HZBE}	Byte Disable to High Z		6		7	ns
Write Cycle ^[8]						
t _{WC}	Write Cycle Time	12		15		ns
t _{SCE}	\overline{CE} LOW to Write End	9		10		ns
t _{AW}	Address Set-Up to Write End	8		10		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		10		ns
t _{SD}	Data Set-Up to Write End	6		8		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		6		7	ns
t _{BW}	Byte Enable to End of Write	8		9		ns

Notes:

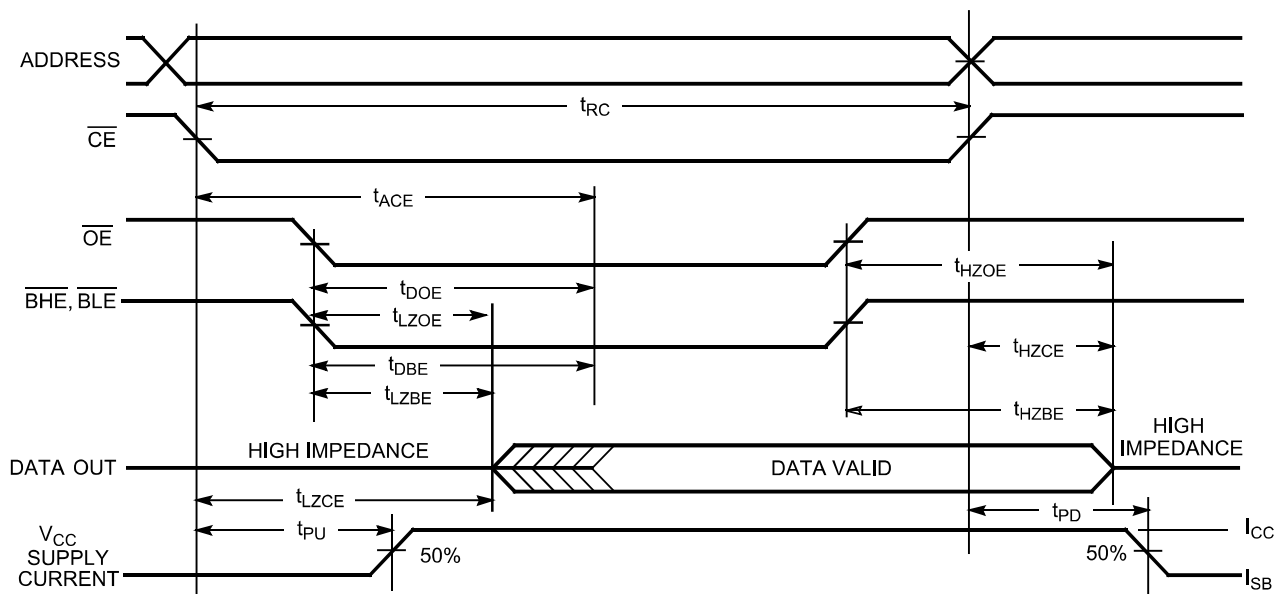
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and BHE / \overline{BLE} LOW. \overline{CE} , \overline{WE} and BHE / \overline{BLE} must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1^[9, 10]



Read Cycle No. 2 (OE Controlled)^[10, 11]

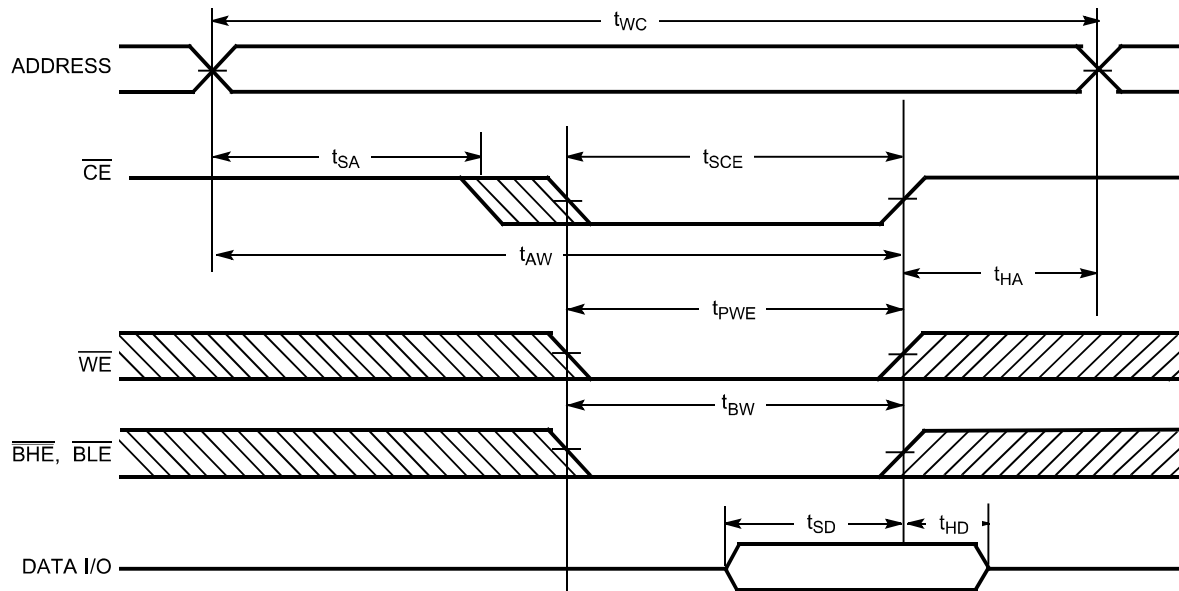


Notes:

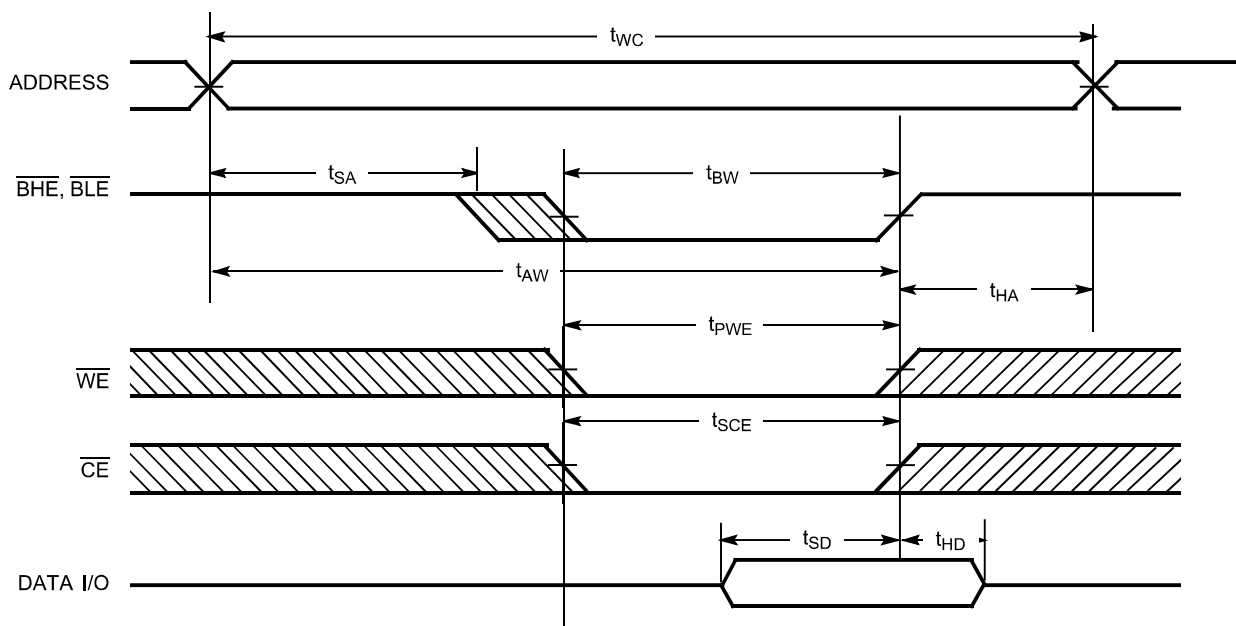
9. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
10. \overline{WE} is HIGH for read cycle.
11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[12, 13]



Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



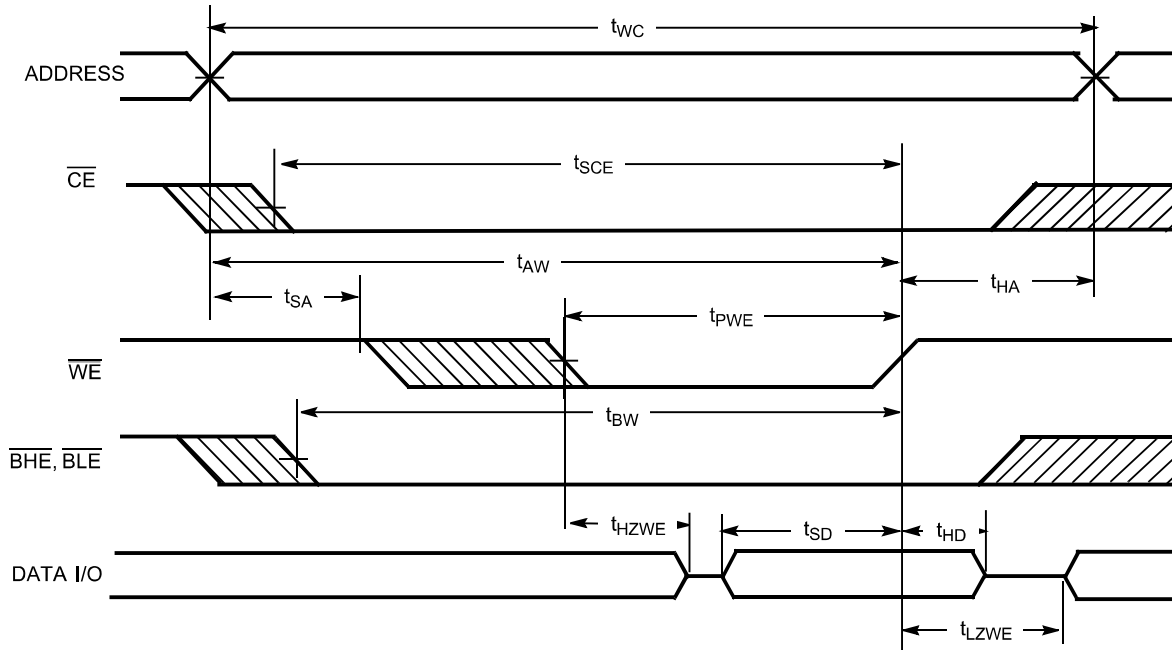
Notes:

12. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.

13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)



Truth Table

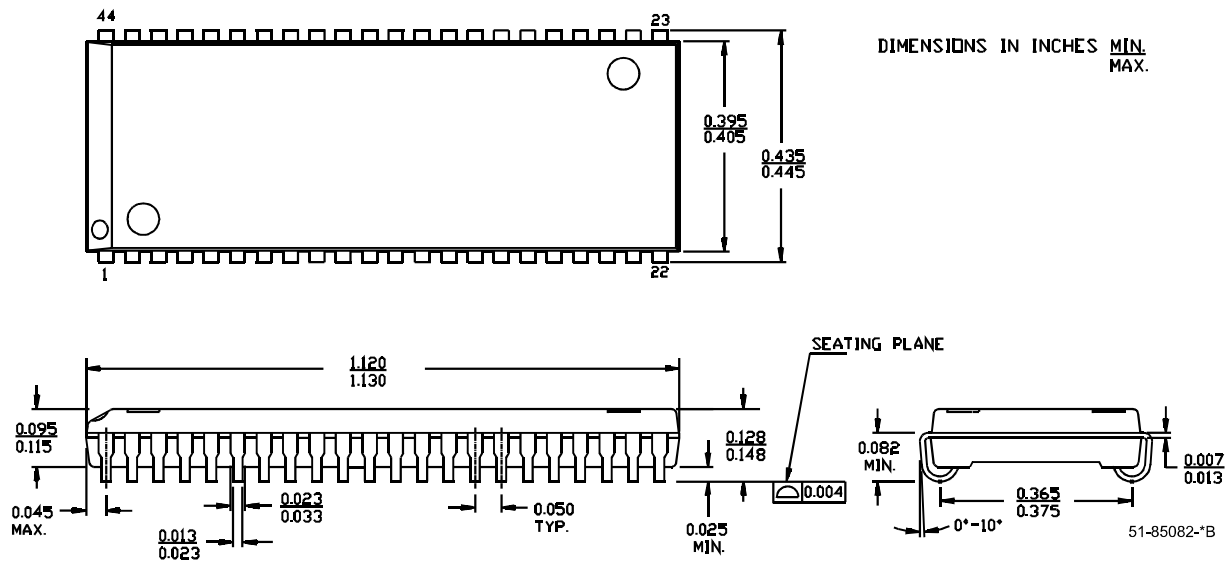
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1020B-12VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1020B-12VXC		44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1020B-12ZC	51-85087	44-pin TSOP Type II	
	CY7C1020B-12ZXC		44-pin TSOP Type II (Pb-free)	
15	CY7C1020B-15ZC	51-85087	44-pin TSOP Type II	
	CY7C1020B-15ZXC		44-pin TSOP Type II (Pb-free)	

Package Diagrams

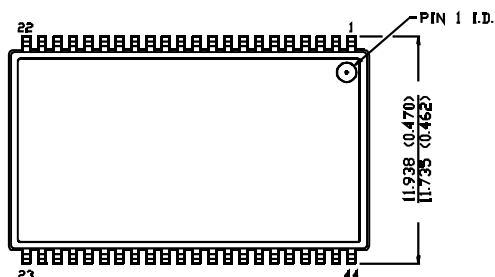
44-pin (400-Mil) Molded SOJ (51-85082)



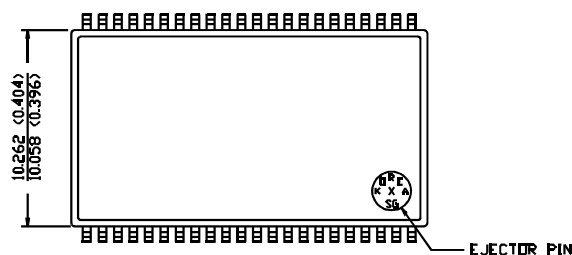
Package Diagrams (continued)

44-pin TSOP II (51-85087)

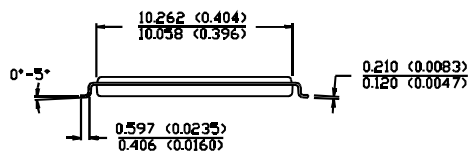
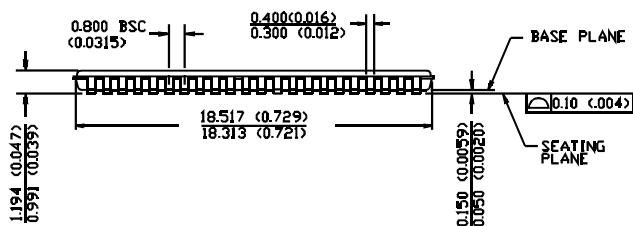
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY7C1020B 32K x 16 Static RAM Document #: 38-05171				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	115439	05/09/02	DSG	New Data Sheet
*A	116869	08/21/02	DFP	Added L-Power Specifications.
*B	426747	See ECN	ZSD	Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court". Added thermal resistance table. Updated the ordering information table and replaced the Package Name column with Package Diagram.
*C	465909	See ECN	NXR	Corrected typo in Pin Configuration (Changed A ₁₅ to A ₄) Removed L-Power Specifications Updated the Ordering Information table