SONY® CXA1114P/M/CXA1434P

Audio Video Switch Compatible with I²C Bus

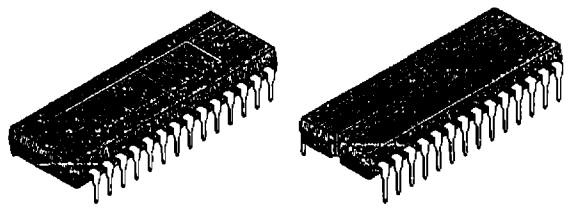
Description

The CXA1114P and CXA1434P are bipolar ICs developed as audio video switches for the I²C bus.

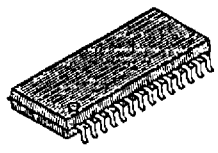
Features

- Serial control through I²C bus
- 4 channels for input and 3 channels for output
- The 3 channels for output are respectively independent and allow for input selection at will
- Video and audio switches are independently controllable
- Corresponds to mutual dubbing and simultaneous broadcasting
- Built-in amplifier with gain = 6 dB for both video and audio systems
- Wide band video amplifier (15 MHz – 3dB)
- Slave address for CXA1114 and CXA1434 differ CXA1114: 90H, CXA1434: 96H

CXA1114P 28pin DIP (Plastic)
CXA1434P



CXA1114M 28pin SOP (Plastic)



Functions

Input channels { Video input 4 channels / Audio input, STEREO 4 channels
Output channels { Video output 3 channels / Audio output, STEREO 3 channels

Each output features a built-in 6dB gain amplifier. Output at the 3 channels can independently select an input at will.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

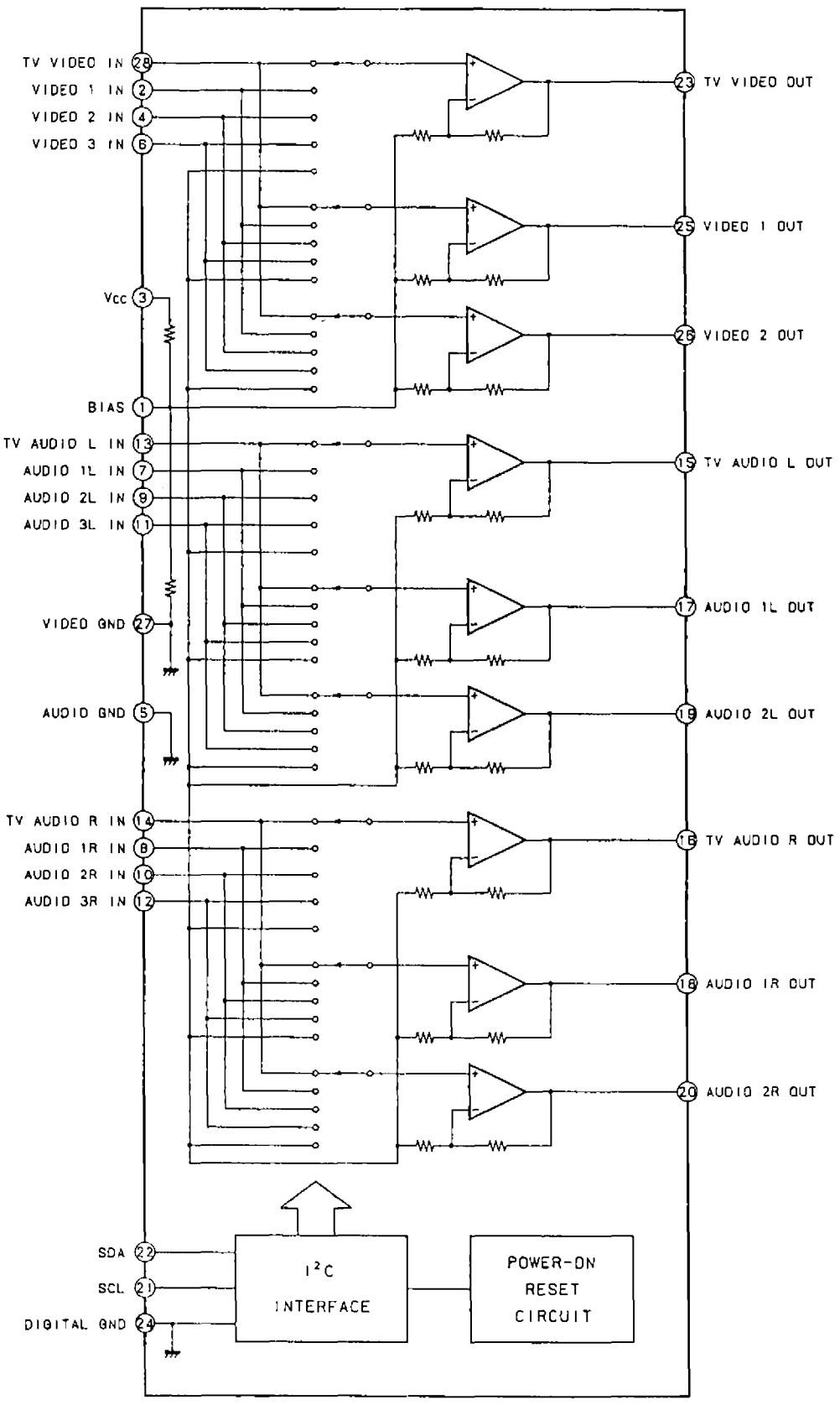
• Supply voltage	Vcc	12	V	
• Operating temperature	Topr	–20 to +75	°C	
• Storage temperature	Tstg	–65 to +150	°C	
• Allowable power dissipation	PD	830	mW	(CXA1114P/CXA1434P)
		570	mW	(CXA1114M)

Operating Supply Voltage Range

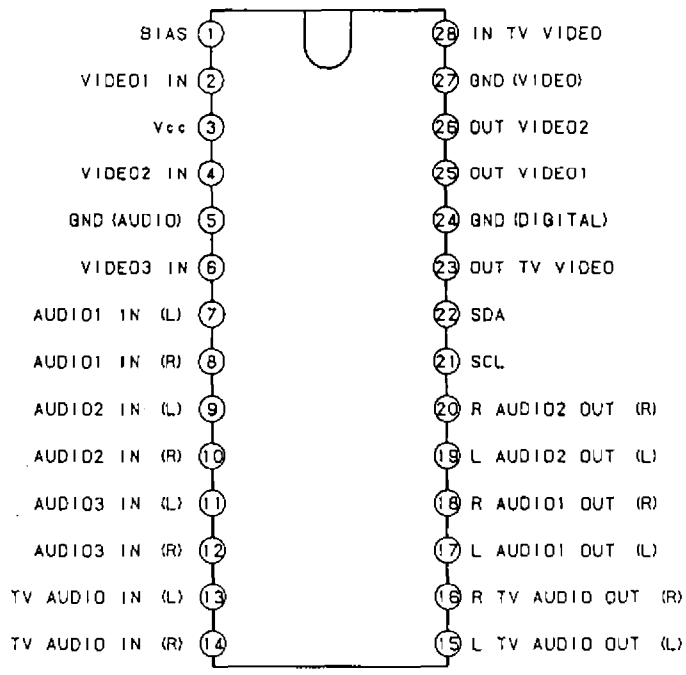
	Vcc	+8 to +10	V

E89864B21-YA

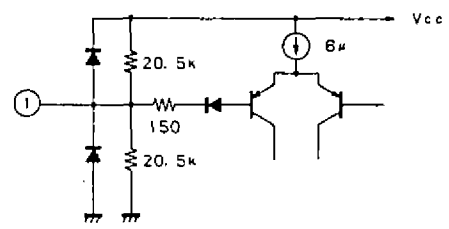
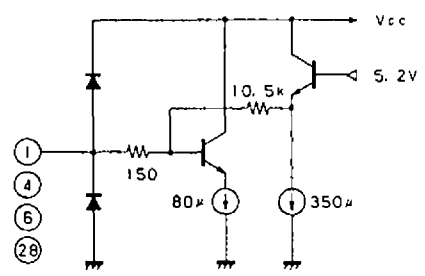
Block Diagram

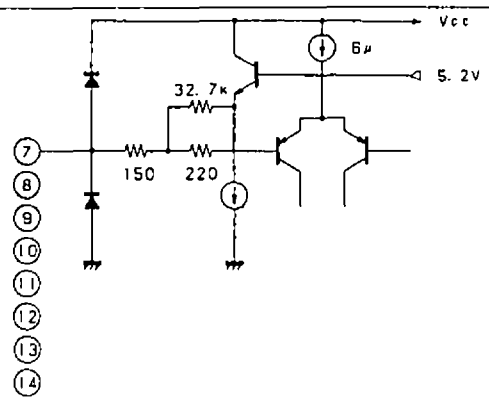
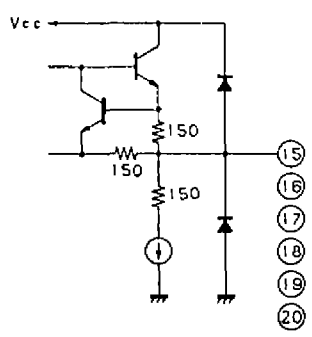
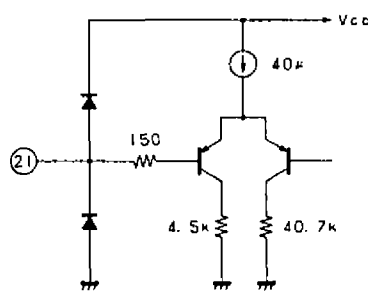
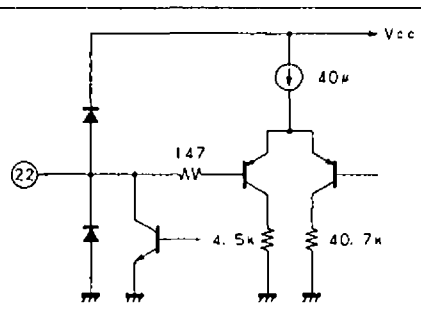


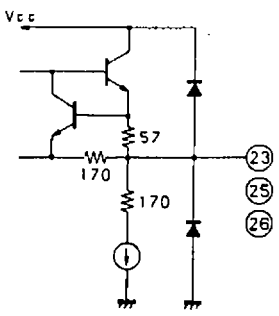
Pin Configuration (Top View)



Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	BIAS	4.6V		Builds up Vcc/2 that becomes the internal bias reference. Supply ripple is suppressed by installing a capacitor. Cut off frequency is supplied through, $f_0 = \frac{1000}{2\pi \times 11 \times C\ (\mu F)}$ [Hz]
2 4 6 28	VIDEO 1 IN VIDEO 2 IN VIDEO 3 IN TV.VIDEO IN	4.5V		Video 1, 2, 3, and TV video input pins
3	Vcc	9.0V		Power supply pin

No.	Symbol	Voltage	Equivalent circuit	Description
5 24 27	GND(AUDIO) GND(DIGITAL) GND(VIDEO)			Audio, digital and video GND pins
7 8 9 10 11 12 13 14	AUDIO 1 IN(L) AUDIO 1 IN(R) AUDIO 2 IN(L) AUDIO 2 IN(R) AUDIO 3 IN(L) AUDIO 3 IN(R) TV AUDIO IN(L) TV AUDIO IN(R)	4.6V		Input pins for 1,2,3 audio, the TV audio and their respective L and R channels
15 16 17 18 19 20	TV AUDIO OUT(L) TV AUDIO OUT(R) AUDIO 1 OUT(L) AUDIO 1 OUT(R) AUDIO 2 OUT(L) AUDIO 2 OUT(R)	4.6V		Output pins for 1,2 audio, the TV audio and their respective L and R channels
21	SCL	—		SCL (Serial Clock Line) of I²C bus standards. Threshold level is set to approx. 2.3V.
22	SDA	—		SDA (Serial Data Line) of I²C bus standards. Threshold level is set to approx. 2.3V.

No.	Symbol	Voltage	Equivalent circuit	Description
23 25 26	TV VIDEO OUT VIDEO 1 OUT VIDEO 2 OUT	4.5V		Output pins for TV video, video 1 and video 2.

Electrical Characteristics (Ta=25°C, Vcc=9V See Fig. 1 to 10)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Consumption current	Icc	Vcc=9V, No signal, No load (Fig.1)	20	35	50	mA
BIAS	Vcc/2	Vcc=9V, No signal, No load	4.2	4.6	5.0	V

(Video system)

I/O pin voltage	Vvpin	Vcc=9V, No signal, No load	4.1	4.5	4.9	V
Frequency characteristics	Fbwv	With input at 0.3 Vp-p and output at 100 kHz set to 0 dB. Test input frequency when output level reaches –3 dB. (Fig.2)	10	15	—	MHz
Gain	GVv	f=100kHz, 0.3Vp-p input (Fig.2)	5.5	6.0	6.5	dB
Input dynamic range	Vdv	At 100 kHz max input level when distortion < 1.0% (Fig.2)	2.0	3.0	—	Vp-p
Crosstalk between video outputs	Vctv	f=4.43MHz, 1Vp-p input (Fig.2)	—	–55	–50	dB
Input resistance	Rinv	Tested at DC (Fig.5)	7	11	15	kΩ
Ripple rejection ratio	RRv	f=100Hz, 0.3Vp-p added to Vcc (Fig.7)	—	–35	–30	dB
Output impedance	Rov	f=100kHz, 5Vp-p input (Fig.3)	—	12	30	Ω

(Audio system)

I/O pin voltage	$V_A$pin	Vcc=9V, no signal, No load	4.4	4.6	4.7	V
Frequency characteristics	Fbw_A	With 1Vp-p input, 1kHz output as 0dB, an input frequency where –3dB is obtained. (Fig.9)	100	—	—	kHz
Gain	Gv_A	f=1kHz, 1Vp-p input (Fig.9)	5.5	6.0	6.5	dB
Total harmonic distortion	THD	f=1kHz, 2.2Vp-p input (Fig.8)	—	0.06	0.2	%
Input dynamic range	Vd_A	At 1 kHz max input level when distortion < 1.0% (Fig.9)	2.8	3.0	—	Vp-p
Crosstalk between audio outputs	Vct_A	f=1kHz, 1Vp-p input (Fig.9)	—	–90	–75	dB
Input resistance	Rin_A	Tested at DC (Fig.6)	25	30	40	KΩ
Ripple rejection ratio	RR_A	f=100Hz, 0.3Vp-p added to Vcc (Fig.7)	—	–50	–40	dB
Output impedance	Ro_A	f=1kHz, 5Vp-p input (Fig.4)	—	12	30	Ω

Output DC offset	Voff	Offset with regards to mute in respective modes. (Fig.9)	—	6.0	25.0	mV
Residual noise	V_{NA}	f_{CL}=300Hz, f_{CH}=19kHz, 40dB amplifier connected. (Fig.10)	—	0.8	5.0	mV

(Logic system) Fig.11

High level input voltage	V_{IH}		3.0	—	5.0	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	During SDA, 3mA flow in	0	—	0.4	V
Clock frequency	f_{SCL}		0	—	100	kHz
Min. waiting time for data modification	t_{BUF}		4.7	—	—	µs
Min. waiting time for start of data transfer	$t_{HD;STA}$		4.0	—	—	µs
Low level clock pulse width	t_{LOW}		4.7	—	—	µs
High level clock pulse width	t_{HIGH}		4.0	—	—	µs
Min. waiting time for start preparation	$t_{SU;STA}$		4.7	—	—	µs
Min. data hold time	$t_{HD;DAT}$		5	—	—	µs
Min. data preparation time	$t_{SU;DAT}$		250	—	—	ns
Rise time	t_R		—	—	1	µs
Fall time	t_F		—	—	300	ns
Min. stop reparation time	$t_{SU;STO}$		4.7	—	—	µs

Electrical Characteristics Test Circuit

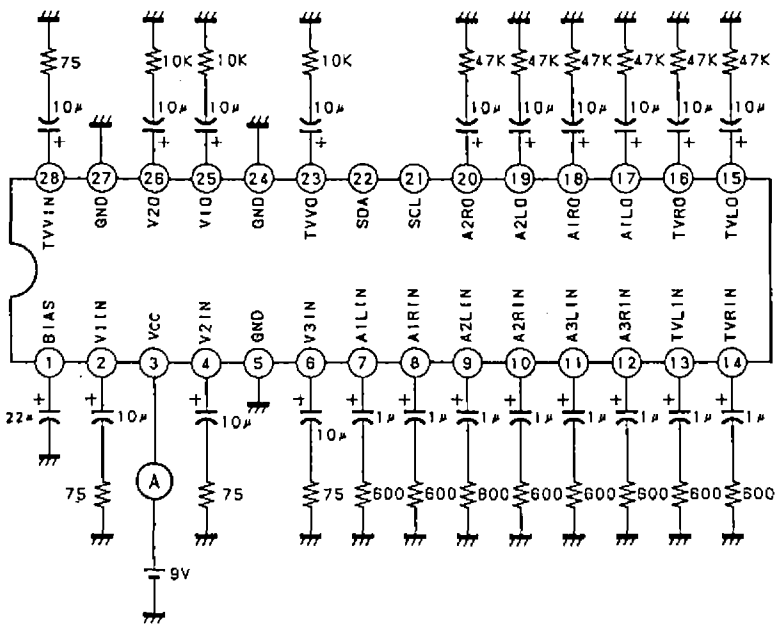


Fig. 1

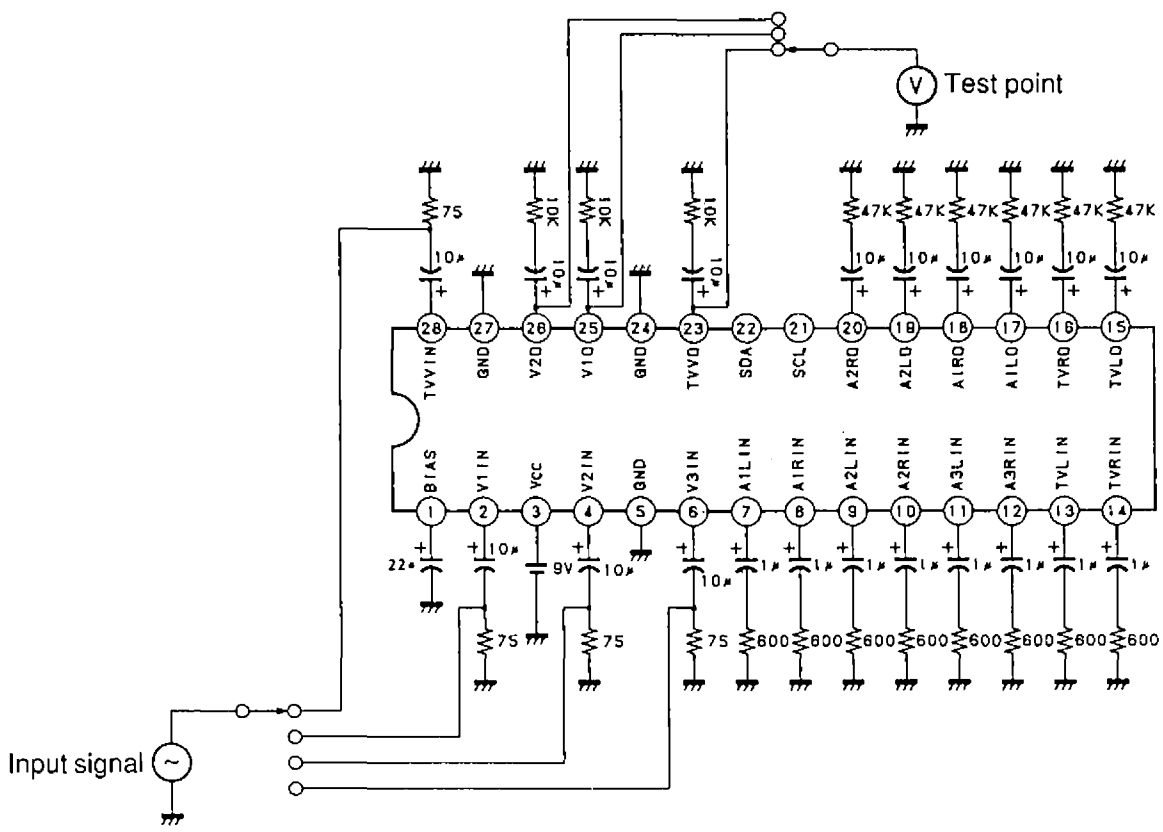


Fig. 2

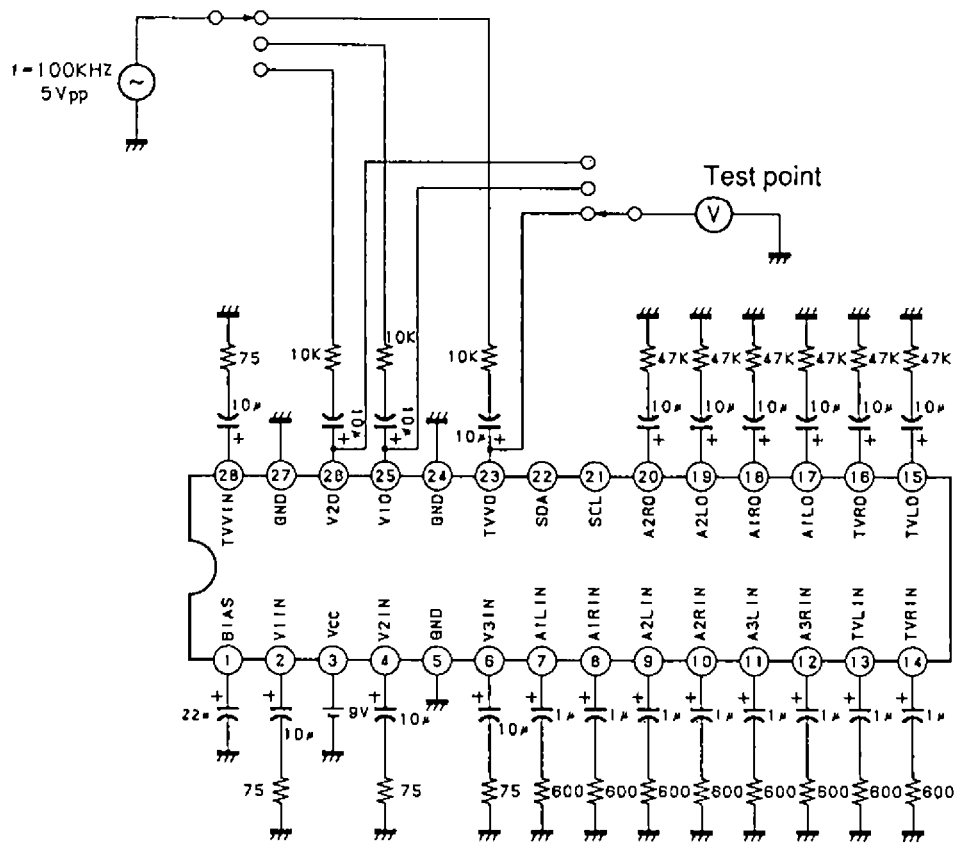

f=100KHz
5Vpp
Test point
V
75
10K
47K
10μ
1μ
600
8V
22μ
TVVIN
GND
V2O
V1O
GND
TVVD
SDA
SCL
A2RO
A2LO
A1RO
A1LO
TVRO
TVLO
BIAS
V1IN
VCC
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN

Fig. 3

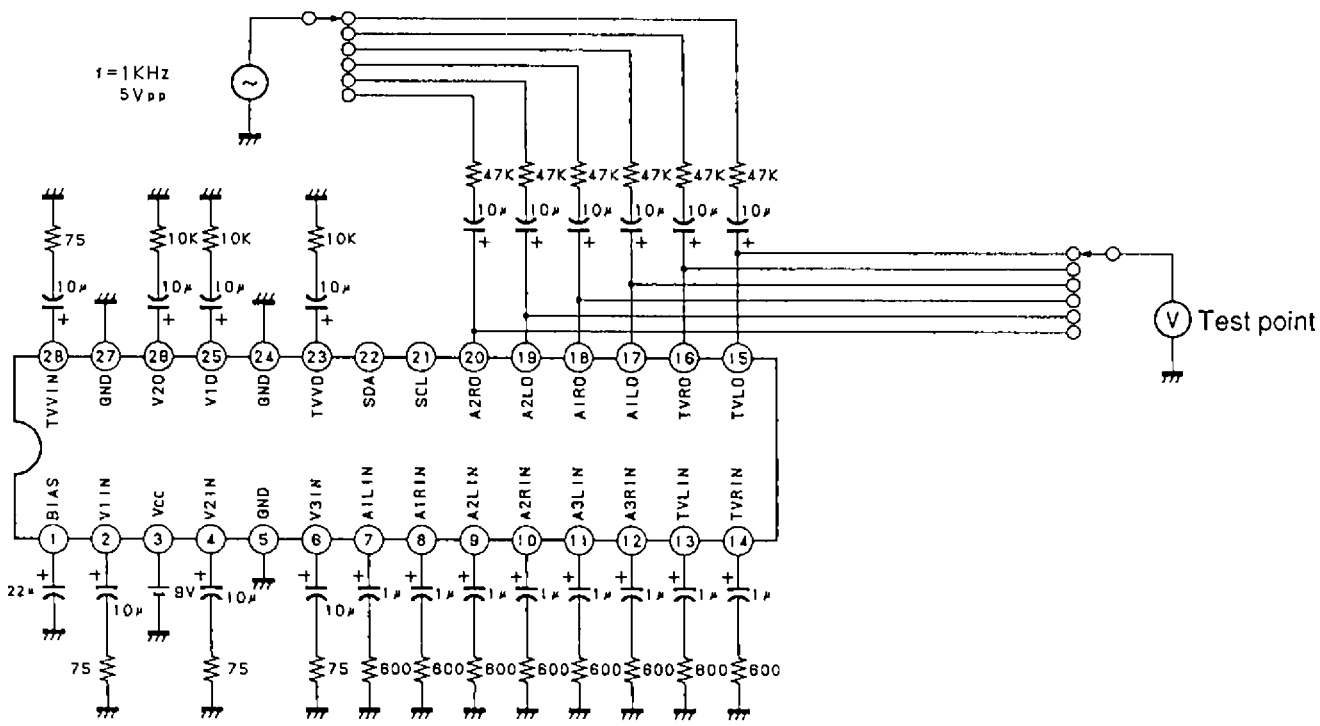

f=1KHz
5Vpp
Test point
V
75
10K
47K
10μ
1μ
600
8V
22μ
TVVIN
GND
V2O
V1O
GND
TVVD
SDA
SCL
A2RO
A2LO
A1RO
A1LO
TVRO
TVLO
BIAS
V1IN
VCC
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN

Fig. 4

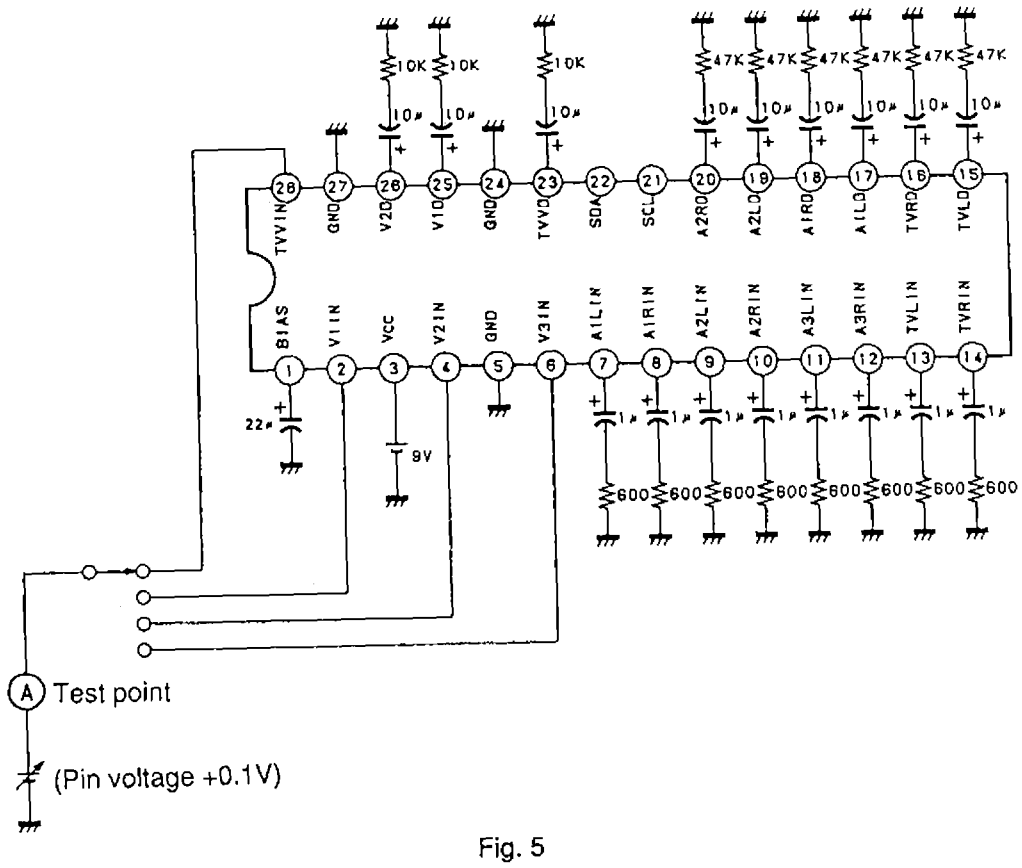

10K
10µ
47K
TVVIN
GND
V2D
V1D
GND
TVVD
SDA
SCL
A2RD
A2LD
A1RD
A1LD
TVRD
TVLD
BIAS
V1IN
VCC
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN
22µ
1µ
9V
600
A
Test point
(Pin voltage +0.1V)

Fig. 5

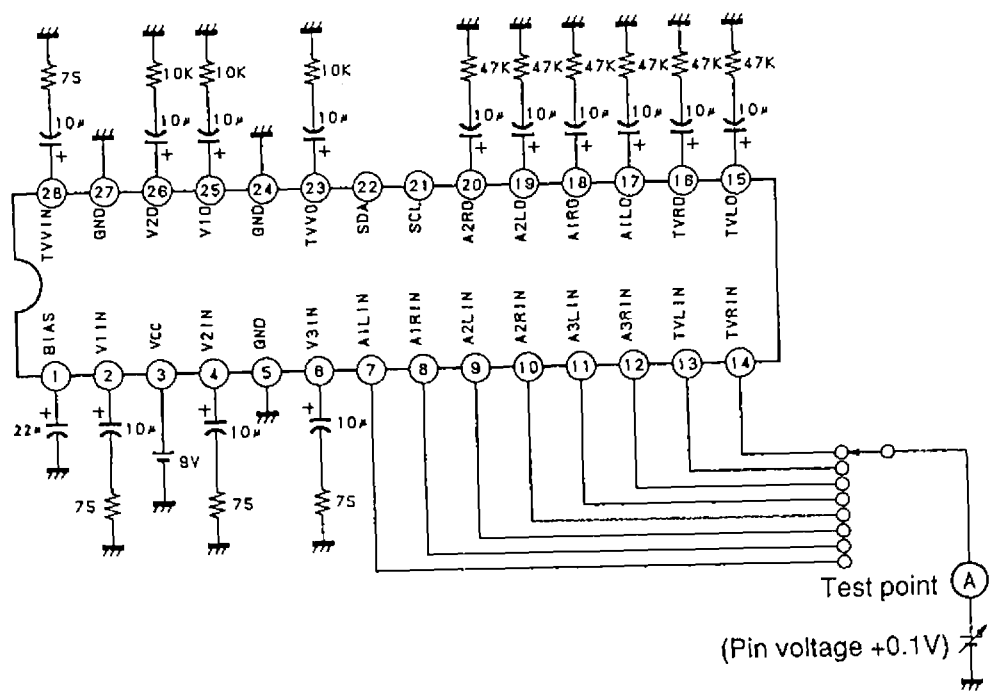

75
10K
10µ
47K
TVVIN
GND
V2D
V1D
GND
TVVD
SDA
SCL
A2RD
A2LD
A1RD
A1LD
TVRD
TVLD
BIAS
V1IN
VCC
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN
22µ
9V
A
Test point
(Pin voltage +0.1V)

Fig. 6

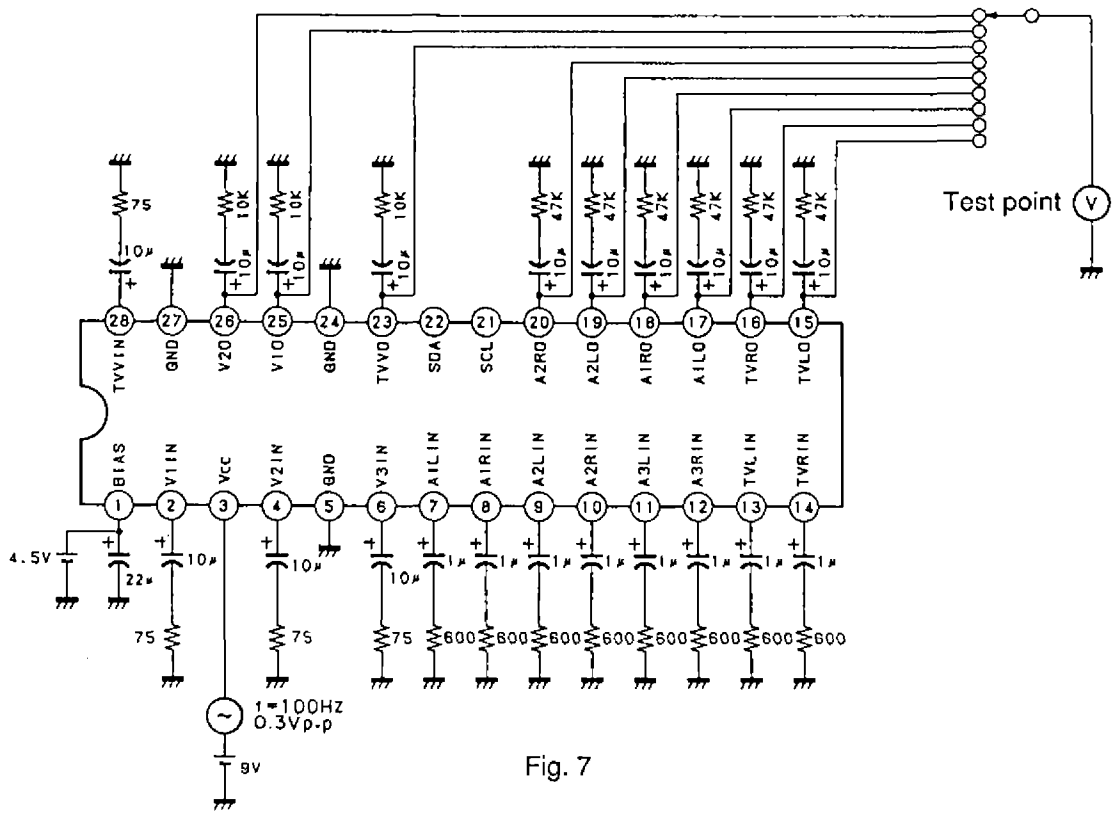

Test point
TVVIN
GND
V2O
V1O
GND
TVVD
SDA
SCL
A2RO
A2LO
A1RO
A1LO
TVRO
TVLO
BIAS
V1IN
Vcc
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN
4.5V
1=100Hz
0.3Vp-p
9V

Fig. 7

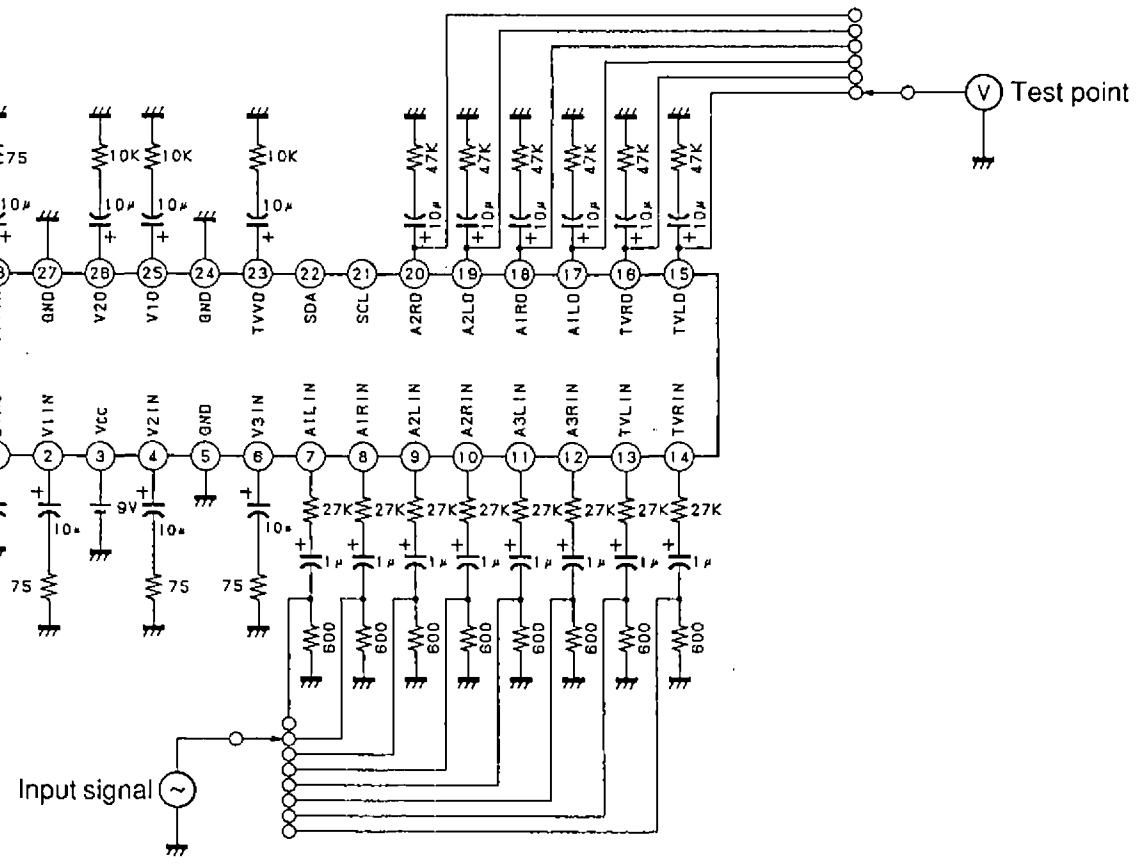

Test point
TVVIN
GND
V2O
V1O
GND
TVVD
SDA
SCL
A2RO
A2LO
A1RO
A1LO
TVRO
TVLO
BIAS
V1IN
Vcc
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN
9V
Input signal

Fig. 8

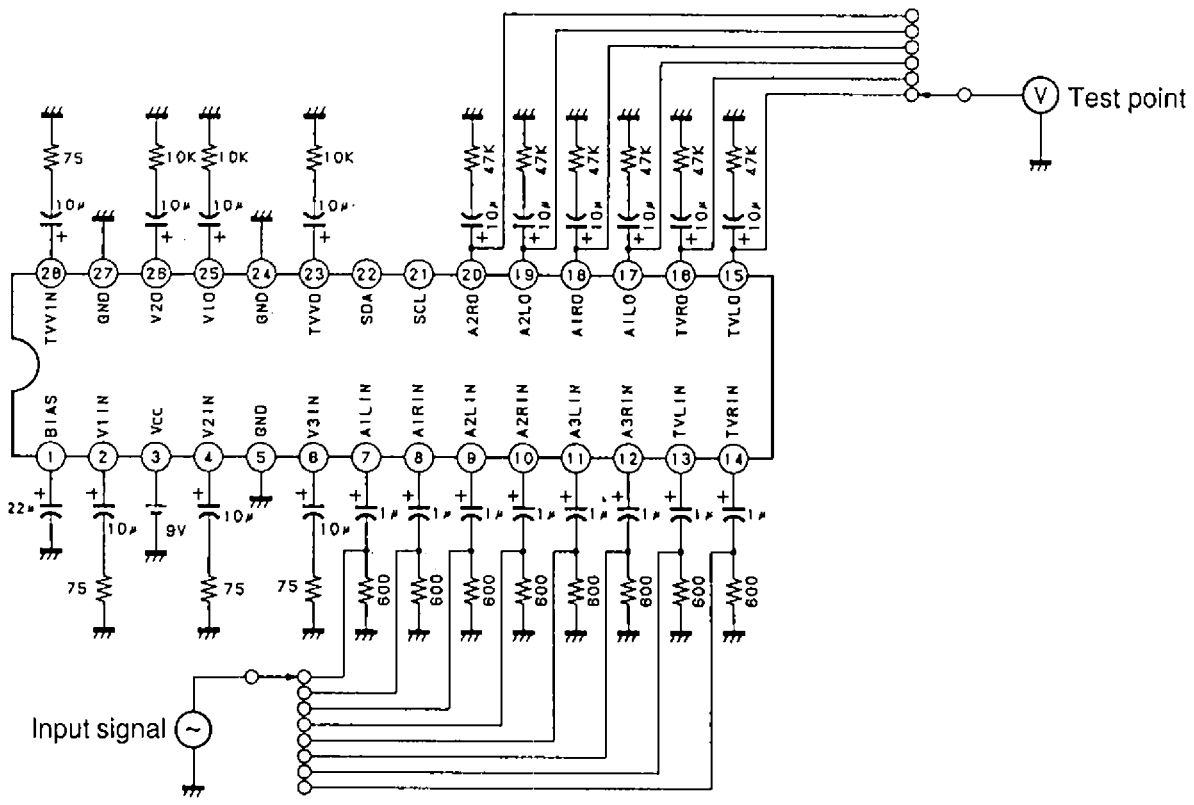

TVV1N
GND
V2O
V1O
GND
TVVO
SDA
SCL
A2RO
A2LO
A1RO
A1LO
TVRO
TVLO
BIAS
V1IN
Vcc
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN
75
10K
47K
600
10µ
1µ
22µ
9V
Input signal
Test point

Fig. 9

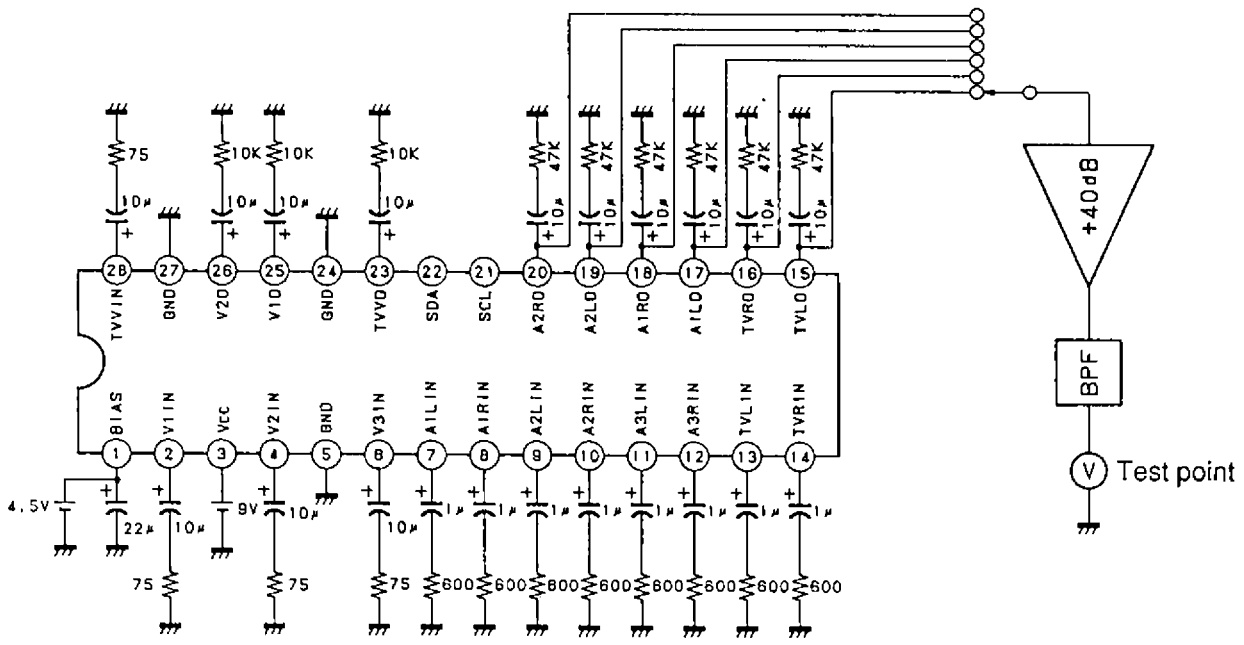

TVV1N
GND
V2O
V1O
GND
TVVO
SDA
SCL
A2RO
A2LO
A1RO
A1LO
TVRO
TVLO
BIAS
V1IN
Vcc
V2IN
GND
V3IN
A1LIN
A1RIN
A2LIN
A2RIN
A3LIN
A3RIN
TVLIN
TVRIN
75
10K
47K
600
10µ
1µ
22µ
9V
4.5V
+40dB
BPF
Test point

Fig. 10

I²C BUS Control signal

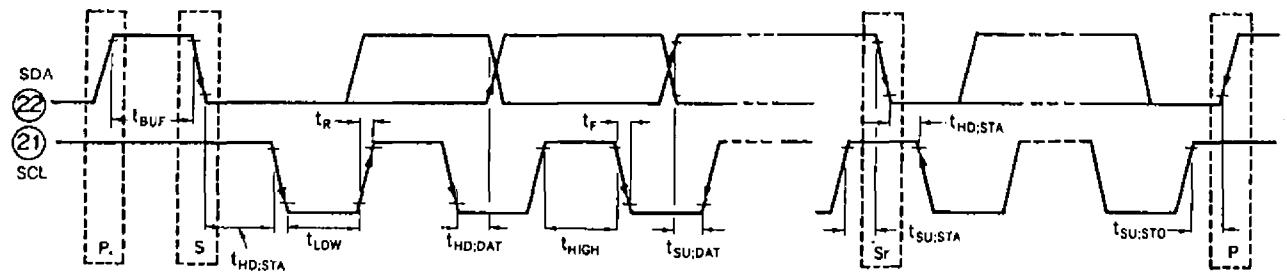


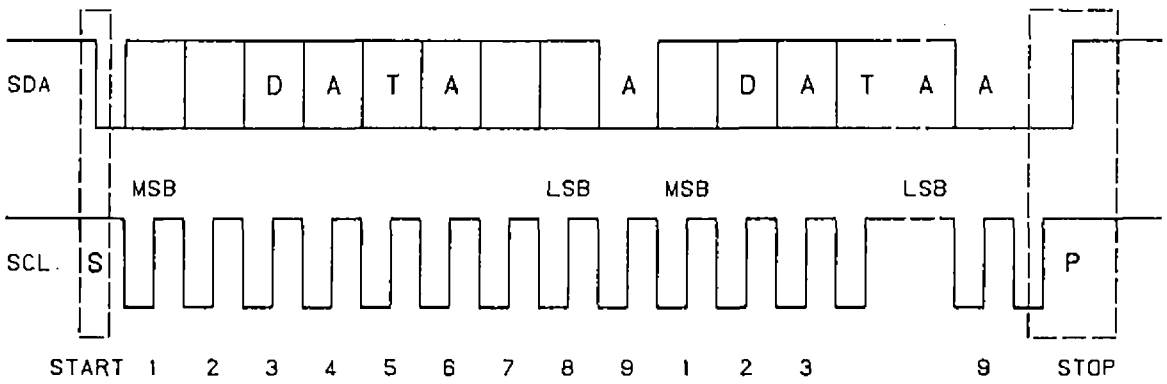
Fig. 11

Operation

The CXA1114 and CXA1434 are used for audio and video selection. These IC's feature 4 channels for video input, 4 for audio stereo input, 3 channels for video output and 3 for audio stereo output. Respective ouputs have built-in amplifiers of approx. 6dB.
The respective audio and video outputs (L and R channels make a set) can independently select the desired input. This is executed through I²C bus.

1) I²C Bus

The I²C bus (Inter IC bus) is a bus system inside the equipment developed by Philips. Start, Stop, Data transfer, Sync and Collision prevention can be executed through two lines, SDA and SCL. The output of respective ICs is either an open collector or an open drain shaped into a wired OR to form the bus line. The bus signal structure is shown below.



S:Start Condition...High to Low transition of SDA when SCL is at High.
P:Stop Condition...Low to High transition of SDA when SCL is at High.
A:Acknowledge...Reply signal coming from slave.

Data is transferred by MSB first. 8 bits in one unit. After that acknowledge (A) is set on to confirm the signal from slave. Normally slave *1 ICs take in data with the rising edge of SCL while Master *2 ICs change data with the falling edge of SCL. The actual data format of CXA1114 and CXA1434 is shown below.

S	Slave address 90H/96H	A	DATA0	A	DATA1	A	DATA2	A	P

Slave address is proper to the IC and is assigned to each IC according to its functions. From the 8 bits the upper 7 bits are proper addresses while the last bit is allocated to R/W. This R/W bit turns to Read *3 at 1 and Write *4 at 0. For the CXA1114/CXA1434, 90H and 96H are assigned as slave addresses. (Write only as there is no Read mode.)

*1 Slave: ICs controlled by the Master. Normally all ICs except microcomputers are slaves.
*2 Master: Indicates ICs that control, such as microcomputers and the like.
*3 Read: Mode in which Master reads out data from Slave.
*4 Write: Mode in which data is written out from Master to Slave.

2) Control

The CXA1114/CXA1434 control is performed by writing 3 bytes of data into 3 control registers composed of 8 bits (actually 6 bits since 2 bits are empty) that control the output selection of 3 systems. First byte data performs the input selection of TV OUT, second byte data that of VIDEO1 OUT and third byte data that of VIDEO 2OUT, respectively. Slave address for CXA1114/CXA1434 is 90H/96H in write mode only.

S	Slave address 90H/96H	A	DATA0	A	DATA1	A	DATA2	A	P

S: Start condition
A: Acknowledge emitted by slave (CXA1114/CXA1434)
P: Stop condition

Structure of Respective Control Registers (DATA 0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0
×	VM	VS1	VS0	×	AM	AS1	AS0

* b_7, b_3 undefined
* At Power On all bits turn to "0". (Power On Reset function)

Video switch control

VM	VS1	VS0	Output pin
0	×	×	Mute (blanking)
1	0	0	TV VIDEO IN
1	0	1	VIDEO 1 IN
1	1	0	VIDEO2 IN
1	1	1	VIDEO3 IN

Audio switch control

AM	AS1	AS0	Output pin
0	×	×	Mute
1	0	0	TV AUDIO IN
1	0	1	AUDIO1 IN
1	1	0	AUDIO2 IN
1	1	1	AUDIO3 IN

3) Control Data Example

Output pin \ Input selection		Video input	Audio input
TV·Video TV sound	ouptut	Video 1	TV sound
Video 1 Video 1 sound	output	Video 2	Video 1 sound
Video 2 Video 2 sound	output	Video 3	Video 2 sound

To select the above the control codes to be used are

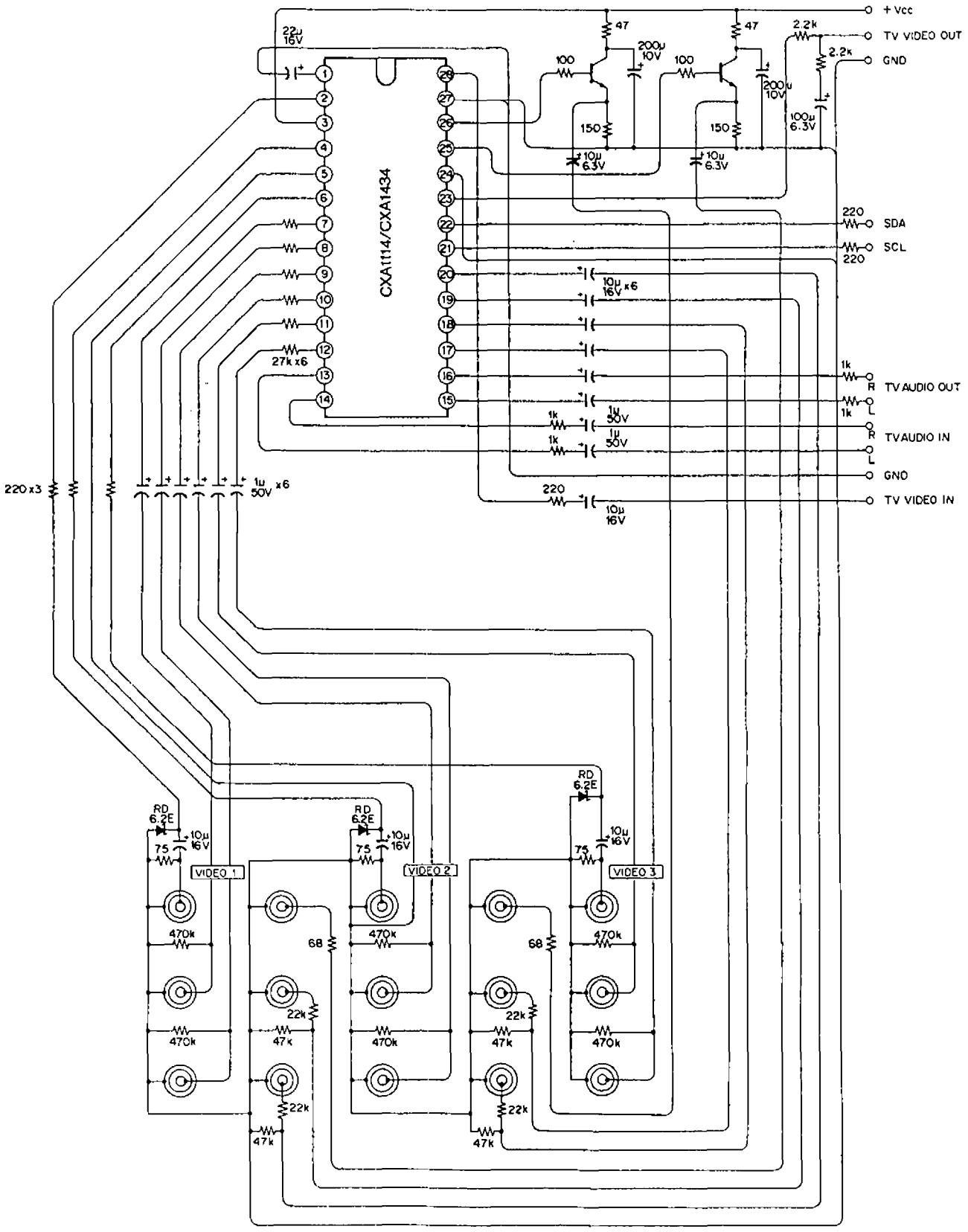
TV·Video TV sound	output	101	100	control code
Video 1 Video 1 sound	output	110	101	
Video 2 Video 2 sound	output	111	110	

For the I²C bus, after the slave adress 90H/96H for CXA1114/ CXA1434, the 3 bytes data transfer is performed:
(× bit is not defined. Either 1 or 0 will do.)

× 101 × 100 (first byte) × 110 × 101 (second byte) × 111 × 110 (third byte)

That is for CXA1114 90H, 54H, 65H, 76H (When ×=0)
90H, DCH, EDH, FEH (When ×=1)
or for CXA1434 96H, 54H, 65H, 76H (When ×=0)
96H, DCH, EDH, FEH (When ×=1)
either can be transferred.

Application Circuit



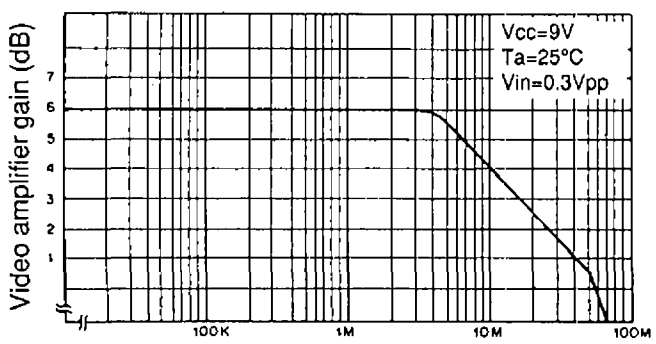
Notes on Operations

As these ICs utilize video, audio and digital signals, the following points should be taken into consideration.

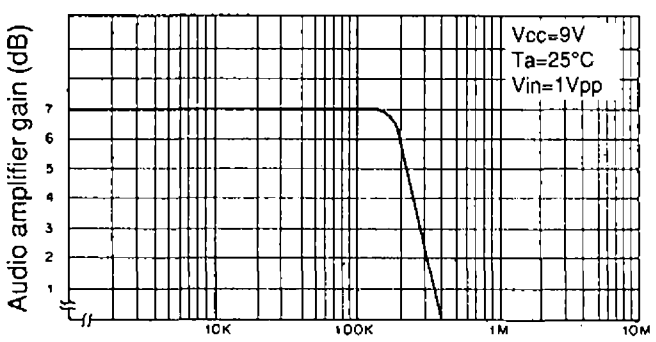
1) On both video and audio systems, the wiring may cause crosstalk. An effective measure would be to separate input by using an earth line on the P.C.B.
2) When control is performed through I²C bus, once it is set on, as long as there is no change in the data (with Power OFF, it is called off however), the condition at which it is set, is kept on. To avoid noise caused by SCL, SDA clocks and data transfer, it is recommended to temporarily stop the master, except during input selection.
3) Pin 1 provides bias. By installing a capacitor here and effective suppression of power supply ripple is obtained.
   Here the cut off frequency obtained is $f_0 = \frac{1000}{2\pi \times 11 \times C\,(\mu F)}$ [Hz]
4) Keep the bypass capacitor for the power supply near Pin 3.

Characteristics Diagram

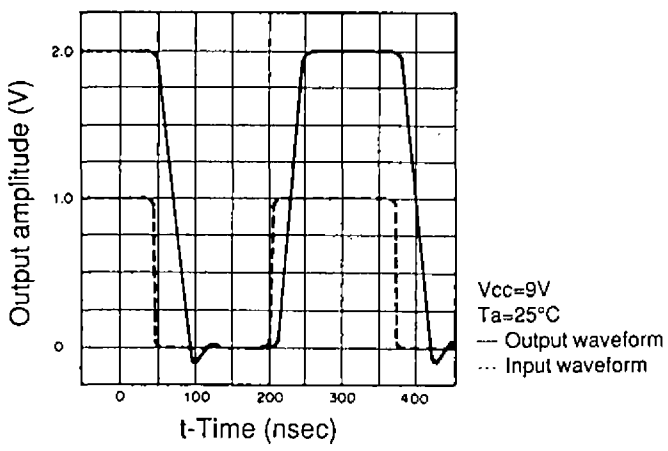
Video amplifier gain vs. Frequency



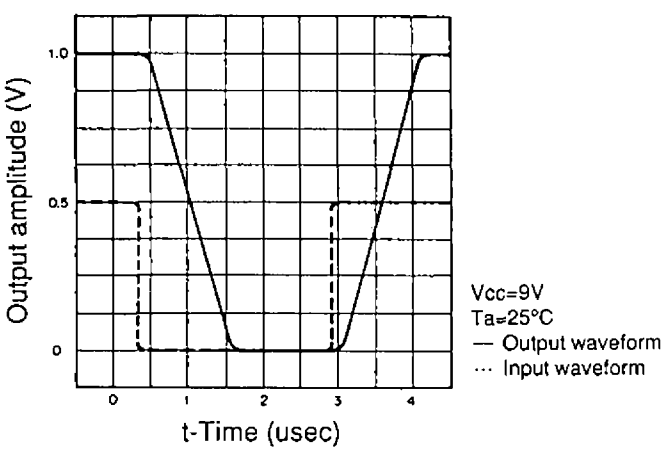
Audio amplifier gain vs. Frequency



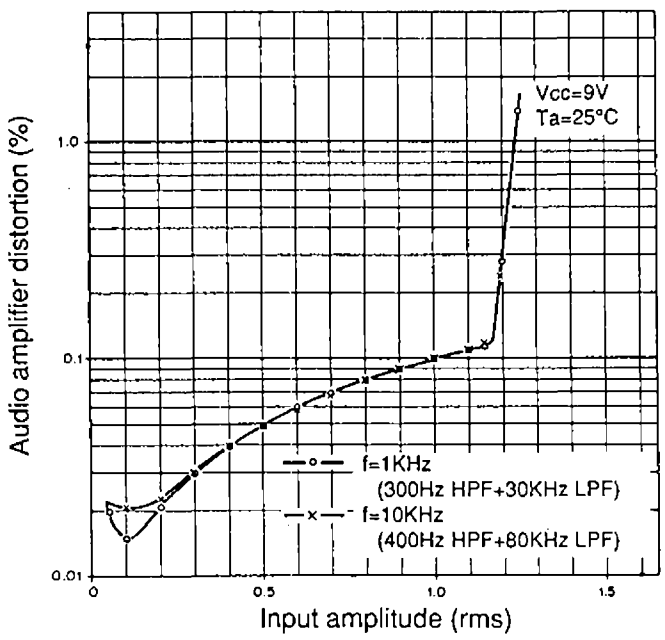
Video amplifier output vs. Rectangular wave input



Audio amplifier output vs. Rectangular wave input



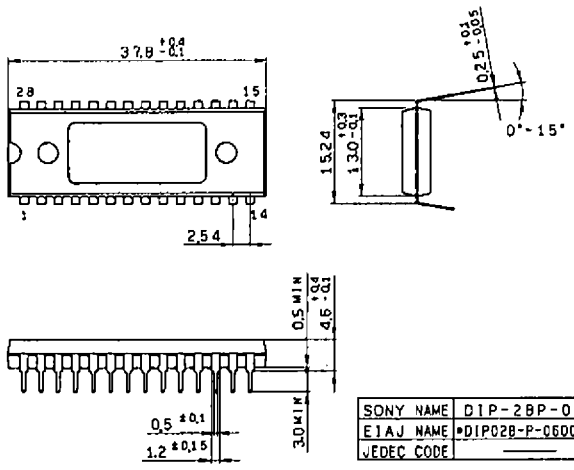
Audio amplifier distortion vs. Input amplitude



Package Outline Unit: mm

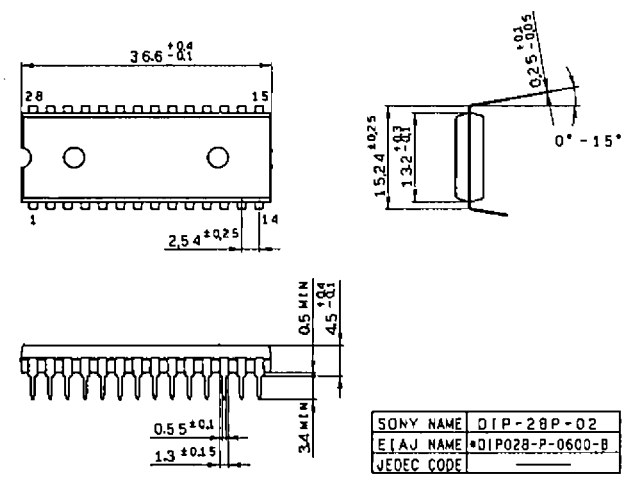
CXA1114P
CXA1434P

28pin DIP (Plastic) 600mil 4.2g



SONY NAME	DIP-28P-03
EIAJ NAME	*DIP028-P-0600-C
JEDEC CODE	———

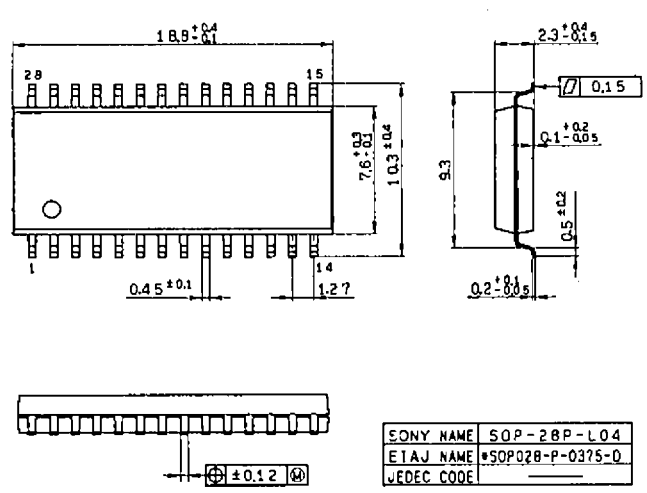
28pin DIP (Plastic) 600mil 4.0g



SONY NAME	DIP-28P-02
EIAJ NAME	*DIP028-P-0600-B
JEDEC CODE	———

CXA1114M

28pin SOP (Plastic) 375mil 0.7g



SONY NAME	SOP-28P-L04
EIAJ NAME	*SOP028-P-0375-D
JEDEC CODE	———

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