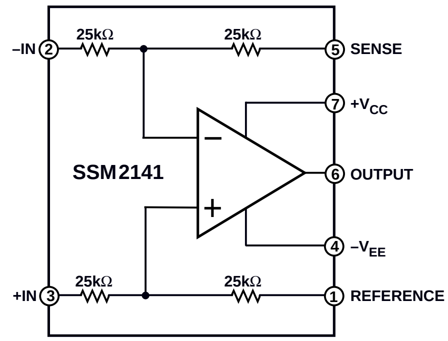
High Common-Mode Rejection Differential Line Receiver

SSM2141

FEATURES
High Common-Mode Rejection
DC: 100 dB typ
60 Hz: 100 dB typ
20 kHz: 70 dB typ
40 kHz: 62 dB typ
Low Distortion: 0.001% typ
Fast Slew Rate: 9.5 V/μs typ
Wide Bandwidth: 3 MHz typ
Low Cost
Complements SSM2142 Differential Line Driver

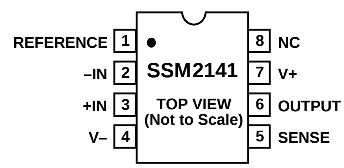
APPLICATIONS
Line Receivers
Summing Amplifiers
Buffer Amplifiers–Drives 600 Ω Load

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

8-Pin Plastic Mini-DIP (P Suffix) Narrow Body SO (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The SSM2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM2141 typically achieves 100 dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40 dB of CMR—inadequate for high-performance audio.

The SSM2141 achieves low distortion performance by maintaining a large slew rate of 9.5 V/μs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM2141 complements the SSM2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM2141 include summing signals, differential preamplifiers, and 600 Ω low distortion buffer amplifiers. For similar performance with G = 1/2, see SSM2143.

REV. C

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Tel: 617/329-4700 Fax: 781/461-3113

SSM2141–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±18 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	SSM2141 Min	Typ	Max	Units
OFFSET VOLTAGE	V_{OS}	V_{CM} = 0 V	–1000	25	1000	µV
GAIN ERROR		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.001	0.01	%
INPUT VOLTAGE RANGE	IVR	(Note 1)	±10			V
COMMON-MODE REJECTION	CMR	V_{CM} = ±10 V	80	100		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±6 V to ±18 V		0.7	15	µV/V
OUTPUT SWING	V_O	R_L = 2 kΩ	±13	±14.7		V
SHORT-CIRCUIT CURRENT LIMIT	I_{SC}	Output Shorted to Ground	+45/–15			mA
SMALL-SIGNAL BANDWIDTH (–3 dB)	BW	R_L = 2 kΩ		3		MHz
SLEW RATE	SR	R_L = 2 kΩ	6	9.5		V/µs
TOTAL HARMONIC DISTORTION	THD	R_L = 100 kΩ R_L = 600 Ω		0.001 0.01		%
CAPACITIVE LOAD DRIVE CAPABILITY	C_L	No Oscillation		300		pF
SUPPLY CURRENT	I_{SY}	No Load		2.5	3.5	mA

NOTES
[1]Input Voltage Range Guaranteed by CMR test.
Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ V_S = ±18 V, –40°C ≤ T_A ≤ +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFFSET VOLTAGE	V_{OS}	V_{CM} = 0 V	–2500	200	2500	µV
GAIN ERROR		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.002	0.02	%
INPUT VOLTAGE RANGE	IVR	(Note 1)	±10			V
COMMON-MODE REJECTION	CMR	V_{CM} = ±10 V	75	90		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±6 V to ±18 V		1.0	20	µV/V
OUTPUT SWING	V_O	R_L = 2 kΩ	±13	±14.7		V
SLEW RATE	SR	R_L = 2 kΩ		9.5		V/µs
SUPPLY CURRENT	I_{SY}	No Load		2.6	4.0	mA

NOTES
[1]Input Voltage Range Guaranteed by CMR test.
Specifications subject to change without notice

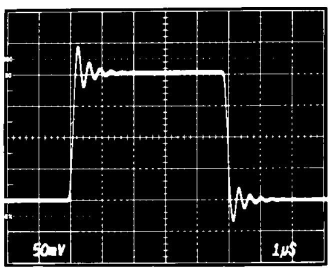
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Input Voltage[1] . . . . Supply Voltage
Output Short-Circuit Duration . . . . Continuous
Storage Temperature Range
  P Package . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . +300°C
Junction Temperature . . . . +150°C
Operating Temperature Range . . . . –40°C to +85°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W

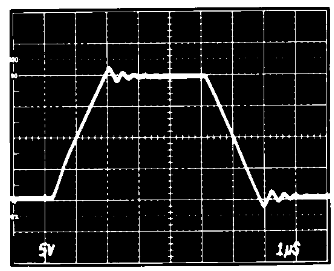
NOTES
[1]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

Typical Performance Characteristics



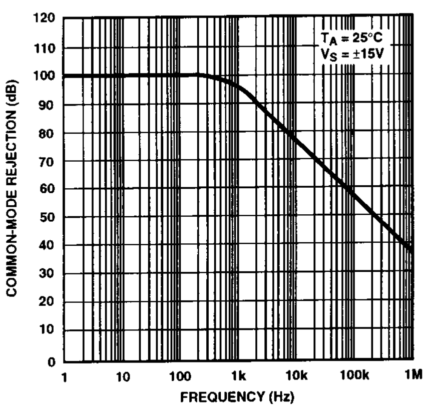
T_A = +25°C
V_S = ±15V

Small Signal Transient Response

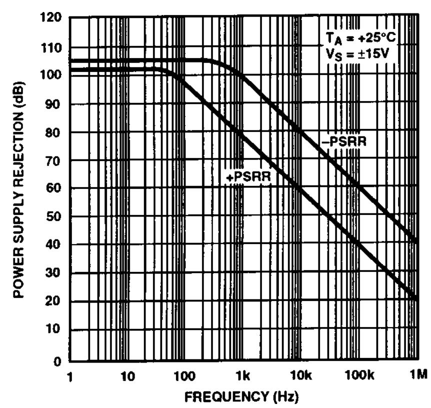


T_A = +25°C
V_S = ±15V

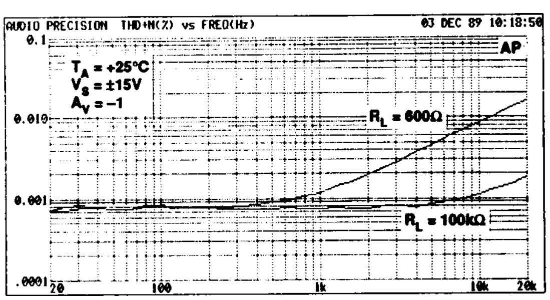
Large Signal Transient Response



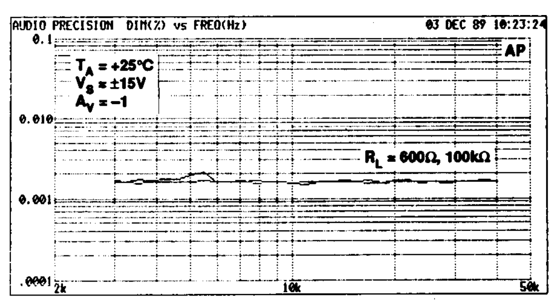
Common-Mode Rejection vs. Frequency



Power Supply Rejection vs. Frequency

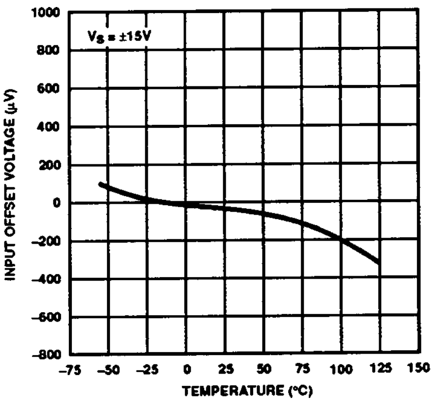


Total Harmonic Distortion vs. Frequency

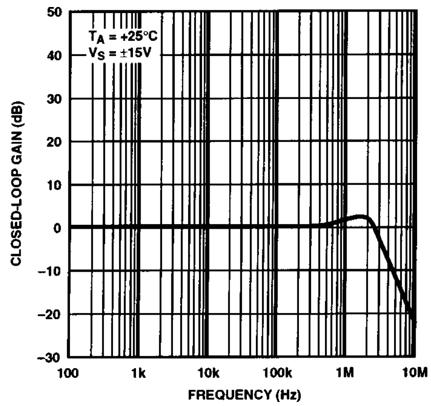


Dynamic Intermodulation Distortion vs. Frequency

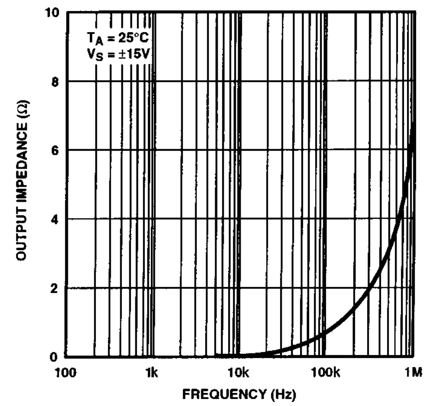
SSM2141–Typical Performance Characteristics



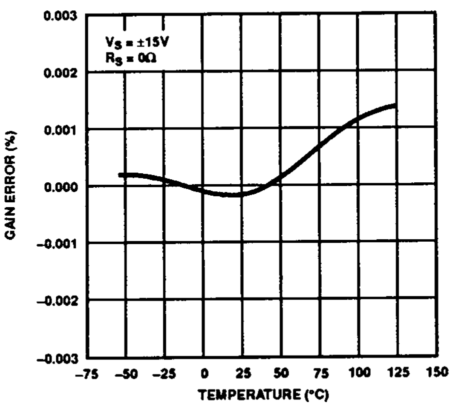
Input Offset Voltage vs. Temperature



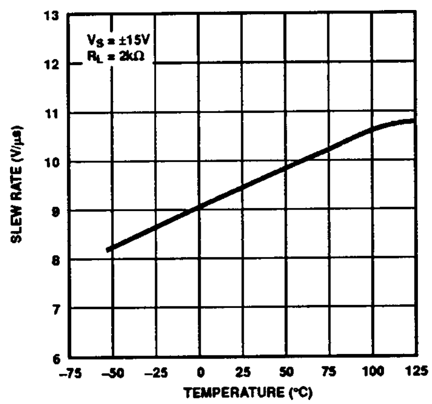
Closed-Loop Gain vs. Frequency



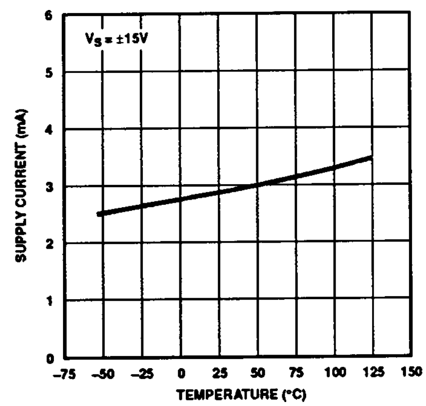
Closed-Loop Output Impedance vs. Frequency



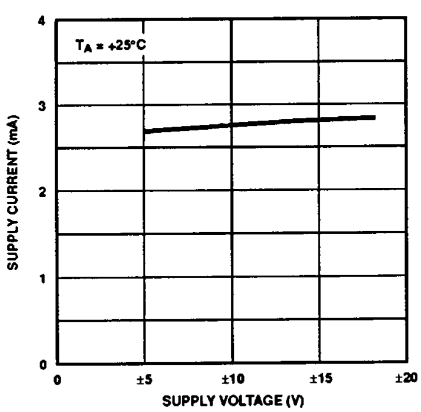
Gain Error vs. Temperature



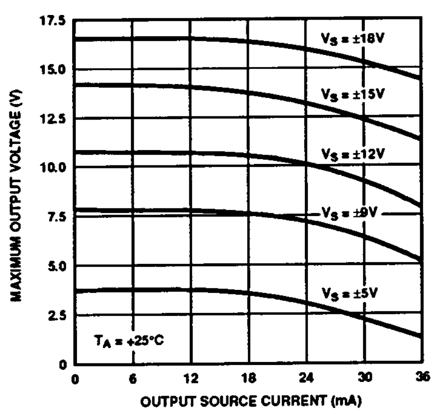
Slew Rate vs. Temperature



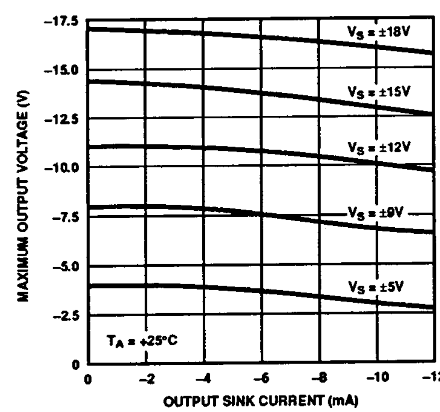
Supply Current vs. Temperature



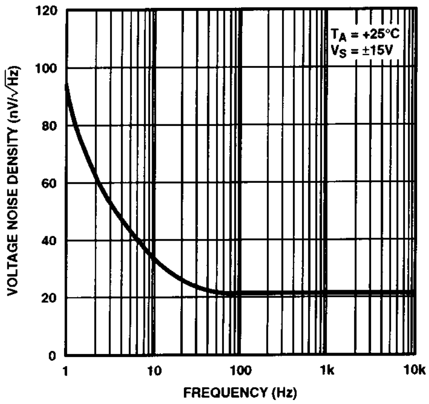
Supply Current vs. Supply Voltage



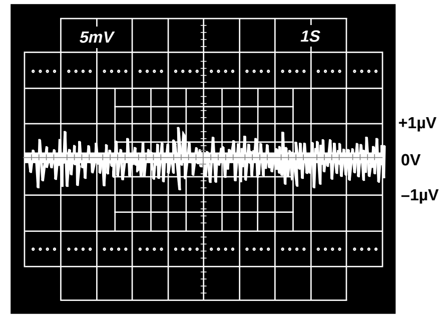
Maximum Output Voltage vs. Output Current (Source)



Maximum Output Voltage vs. Output Current (Sink)

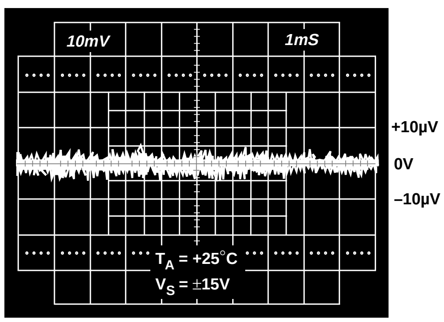


Voltage Noise Density vs. Frequency



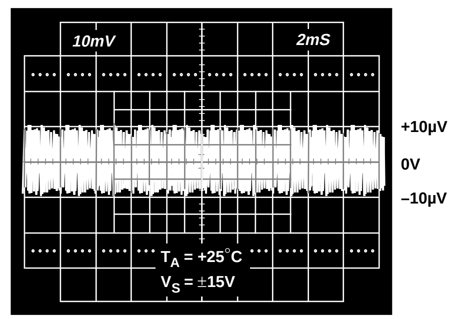
0.1 TO 10Hz PEAK-TO-PEAK NOISE

Low Frequency Voltage Noise



NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10µV/DIV.

Voltage Noise from 0 kHz to 1 kHz

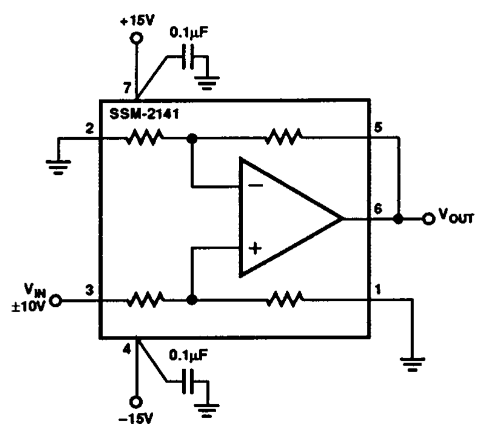


NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10µV/DIV.

Voltage Noise from 0 kHz to 10 kHz

APPLICATIONS INFORMATION

The SSM2141 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. For decoupling, place 0.1 µF capacitor located within close proximity from each supply pin to ground.



Slew Rate Test Circuit

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the SSM2141, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR—even a 5 Ω imbalance will degrade CMR by 20 dB. Also, the matching of the reactive source impedance must be matched in order to preserve the CMRR over frequency.

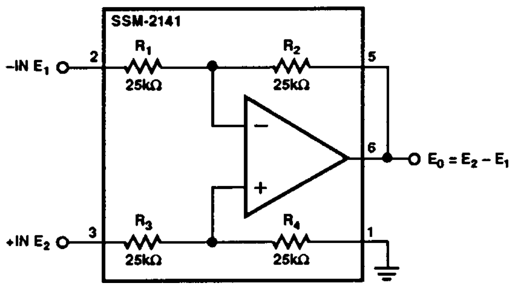


Figure 1. Precision Difference Amplifier. Rejects Common-Mode Signal = $\frac{[E_1+E_2]}{2}$ *by 100 dB*

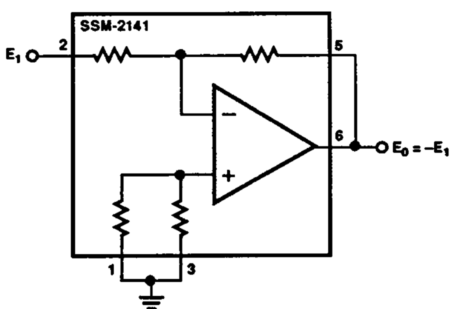


Figure 2. Precision Unity Gain Inverting Amplifier

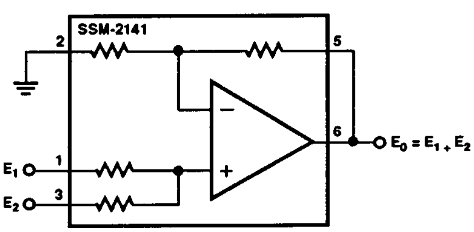


Figure 3. Precision Summing Amplifier

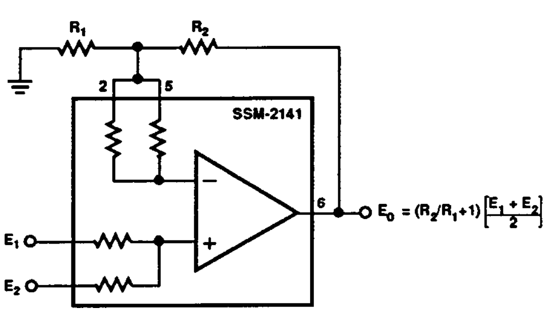


Figure 4. Precision Summing Amplifier with Gain

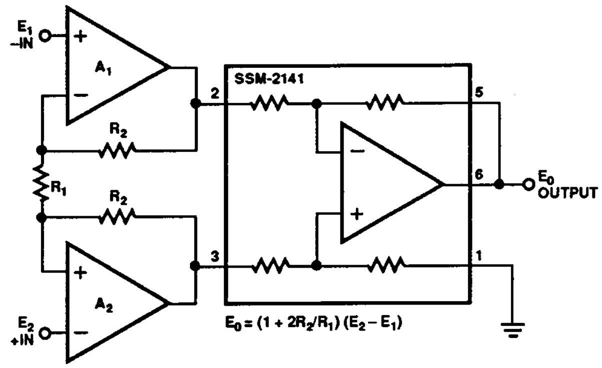
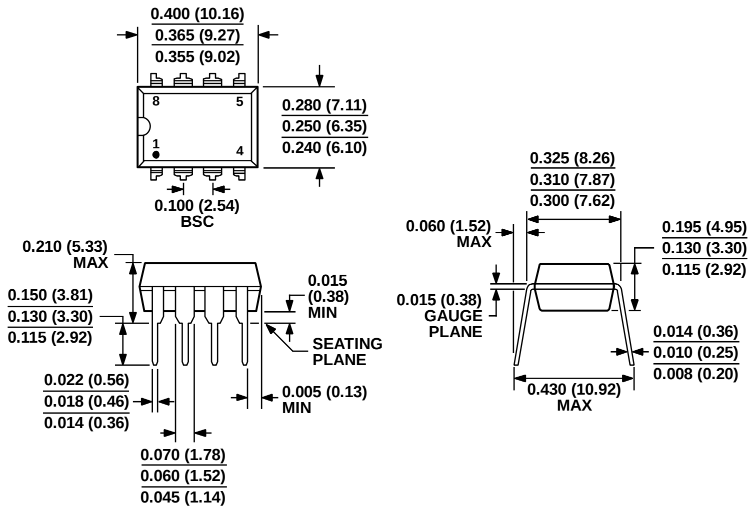


Figure 5. Suitable Instrumentation Amplifier Requirements can be Addressed by Using an Input Stage Consisting of A_1*,* A_2*,* R_1 *and* R_2

OUTLINE DIMENSIONS

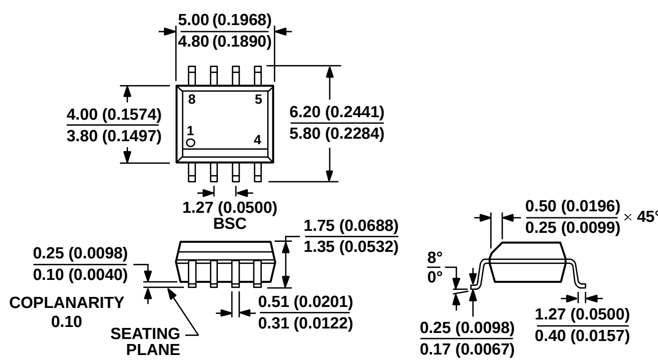


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 6. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 7.8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2141PZ	−40°C ≤ T_A ≤ +85°C	8-Lead PDIP	N-8
SSM2141SZ	−40°C ≤ T_A ≤ +85°C	8-Lead SOIC_N	R-8
SSM2141SZ-REEL	−40°C ≤ T_A ≤ +85°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

REVISION HISTORY

6/11—Rev. B to Rev. C

Updated Outline Dimensions 7
Changes to Ordering Guide 8

5/91—Rev. A to Rev. B

D10008-0-6/11(C)