National Semiconductor

MM55108, MM55110 PLL Frequency Synthesizer with Receive/Transmit Mode

General Description

The MM55108 and MM55110 PLL frequency synthesizers are monolithic metal gate CMOS integrated circuits which contain phase locked loop circuits useful for frequency synthesis applications. The devices operate from a single power supply and contain an oscillator with feedback resistor, divider chain, a binary input programmable divider with control logic for the transmit mode (÷ by (N + 91)), and the necessary phase detector logic. The devices may be used in double IF or single IF systems.

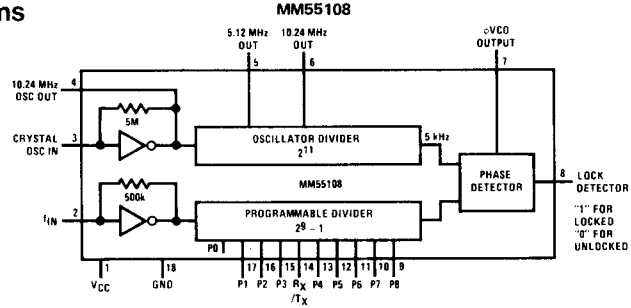
Both the MM55108 and the MM55110 use a 10.24 MHz quartz crystal to determine the reference frequency. The MM55108 has a 2^{11} divider chain which generates a 5 kHz reference frequency. The MM55110 has a selectable 2^{10} or 2^{11} divider chain which gives either a 10 kHz or 5 kHz reference frequency. The selection of reference frequency is made by use of the FS pin. In addition, the MM55110 contains an amplifier for filter applications and an additional input to the programmable divider which allows $2^{10} - 1$ division of the input frequency (f_{IN}) for FM applications. Due to the internal amplifier stage at input frequency input (f_{IN}), the MM55108 and MM55110 may take a 0.5 Vp-p signal at f_{IN} as the input frequency for the programmable divider. Inputs to the programmable divider are standard binary signals. Selection of a channel is accomplished by mechanical switches or by external electronic programming of the programmable divider. The ϕVCO output provides a high level voltage (sources current) when the ϕVCO frequency is lower than the lock frequency, and ϕVCO provides a low level voltage (sinks current) when the ϕVCO frequency is higher than the lock frequency. The ϕVCO output goes to a high impedance state (TRI-STATE®) while in lock mode, and the lock detector output LD also goes to a high state under lock condition.

Features

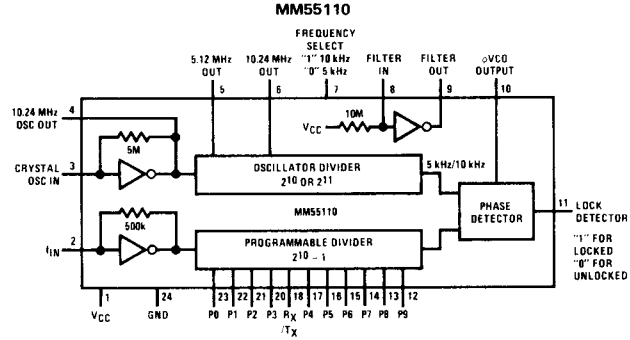
- Single crystal operation
- Single power supply
- Low power CMOS technology
- Binary input channel select code
- 2^{10} or 2^{11} divider chain from oscillator input (MM55110), 2^{11} divider chain (MM55108)
- Buffered 5.12 MHz and buffered 10.24 MHz outputs
- On-chip oscillator with bias resistor
- Pull-down resistors on programmable divider inputs
- Receive/transmit input for ÷ by (N+91) while in transmit mode
- Amplifier for filter applications (MM55110)
- Programmable $2^9 - 1$ division of f_{IN}
- Additional programmable input for $2^{10} - 1$ division of f_{IN} (MM55110)
- Amplifier stage on f_{IN} input to accept 0.5 Vp-p signal

Block Diagrams

MM55108



MM55110



Absolute Maximum Ratings

Voltage at Any Pin	V_{CC} + 0.3V to Gnd − 0.3V
Operating Temperature Range	−30°C to +75°C
Storage Temperature	−40°C to +125°C
Operating V_{CC}	12V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

T_A within operating temperature range, GND = 0V, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		4.5		10.0	V
Supply Current (I_{CC})	Freq. at Osc. In = 10.24 MHz at f_{IN} = 2.5 MHz, All Other I/O Pins Open				
	V_{CC} = 5V		10	15	mA
	V_{CC} = 10V		30	45	mA
Logical "1" Input Voltage ($V_{IN(1)}$)					
P0–P9, FS, R_X/T_X		V_{CC}−0.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
P0–P9, FS, R_X/T_X				0.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
Osc. Out, 10.24 MHz Out, 5.12 MHz Out, LD, ϕVCO, Filter Out	I_{OUT} = −0.5 mA	V_{CC}−0.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
Osc. Out, 10.24 MHz Out, 5.12 MHz Out, LD, ϕVCO, Filter Out	I_{OUT} = 0.5 mA			0.5	V
Logical "1" Input Current ($I_{IN(1)}$)					
Filter In (Pull-Up)	V_{CC} = 4.5V, V_{IN} = 4V	−300		−50	nA
	V_{CC} = 10V, V_{IN} = 9.5V	−500		−100	nA
R_X/T_X (Pull-Up)	V_{CC} = 4.5V, V_{IN} = 4V	−500		−40	µA
	V_{CC} = 10V, V_{IN} = 9.5V	−600		−50	µA
FS, P0–P9 (Pull-Down)	V_{CC} = 4.5V, V_{IN} = 4V	4		40	µA
	V_{CC} = 10V, V_{IN} = 9.5V	20		200	µA
Logical "0" Input Current ($I_{IN(0)}$)					
Filter In (Pull-Up)	V_{CC} = 4.5V, V_{IN} = 0.5V	−600		−100	nA
	V_{CC} = 10V, V_{IN} = 0.5V	−3.0		−0.5	µA
R_X/T_X (Pull-Up)	V_{CC} = 4.5V, V_{IN} = 0.5V	−800		−100	µA
	V_{CC} = 10V, V_{IN} = 0.5V	−5.0		−0.8	mA
FS, P0–P9 (Pull-Down)	V_{CC} = 4.5V, V_{IN} = 0.5V	1		10	µA
	V_{CC} = 10V, V_{IN} = 0.5V	2		30	µA
Maximum Toggle Frequency at f_{IN}	V_{CC} = 5V	3			MHz
	V_{CC} = 7.5V	5			MHz
Input Signal at f_{IN}	Small Signal (AC Coupled) or	0.5			Vp-p
	$V_{IN(1)}$	V_{CC}−0.5			V
	$V_{IN(0)}$			0.5	V
Duty Cycle at f_{IN}		30		70	%
Maximum Osc. Frequency at Osc. In	V_{CC} = 5V, 10.24 MHz Crystal	10.24			MHz
TRI-STATE® Leakage at ϕVCO	V_{OUT} = V_{CC} or Gnd			±1	µA

Typical Applications

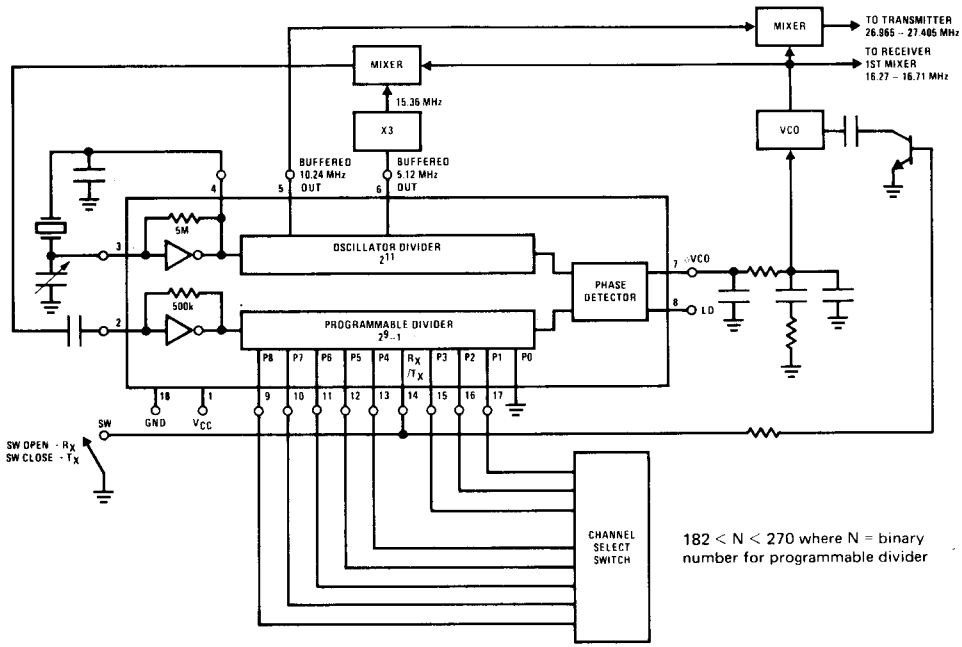


FIGURE 1. MM55108 Single Crystal 40-Channel Low Side Injection

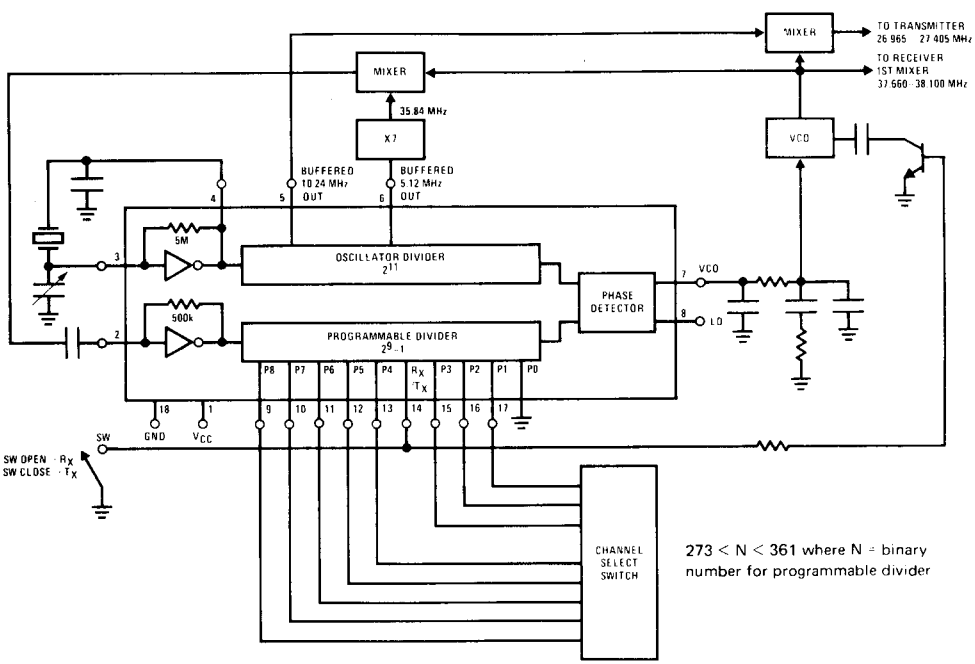


FIGURE 2. MM55108 Single Crystal 40-Channel High Side Injection

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Truth Tables

TABLE I. Binary Inputs to Programmable Divider for MM55108

	R_X/T_X "1" OR "OPEN" N	R_X/T_X "0" OR "CLOSED" N	INPUTS							
			2^8 P8	2^7 P7	2^6 P6	2^5 P5	2^4 P4	2^3 P3	2^2 P2	2^1 P1
	1	92	0	0	0	0	0	0	0	0
	2	93	0	0	0	0	0	0	0	1
	4	95	0	0	0	0	0	0	1	0
	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
Channel 1 →	182	273	0	1	0	1	1	0	1	1
	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
Channel 40 →	270	361	1	0	0	0	0	1	1	1
	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
	510	601	1	1	1	1	1	1	1	1

1 = logical "1"
0 = logical "0"

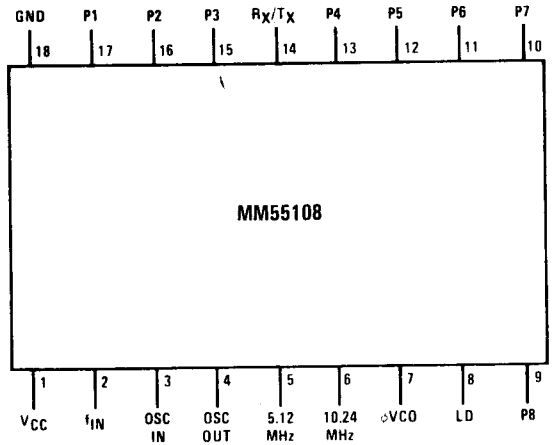
TABLE II. Binary Inputs to Programmable Divider for MM55110

	R_X/T_X "1" OR "OPEN" N	R_X/T_X "0" OR "CLOSED" N	INPUTS									
			2^9 P9	2^8 P8	2^7 P7	2^6 P6	2^5 P5	2^4 P4	2^3 P3	2^2 P2	2^1 P1	2^0 P0
	1	92	0	0	0	0	0	0	0	0	0	X
	2	93	0	0	0	0	0	0	0	0	1	0
	3	94	0	0	0	0	0	0	0	0	1	1
	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.
Channel 1 →	182	273	0	0	1	0	1	1	0	1	1	0
	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.
Channel 40 →	270	361	0	1	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.
	1023	1114	1	1	1	1	1	1	1	1	1	1

X = don't care
1 = logical "1"
0 = logical "0"

Connection Diagrams

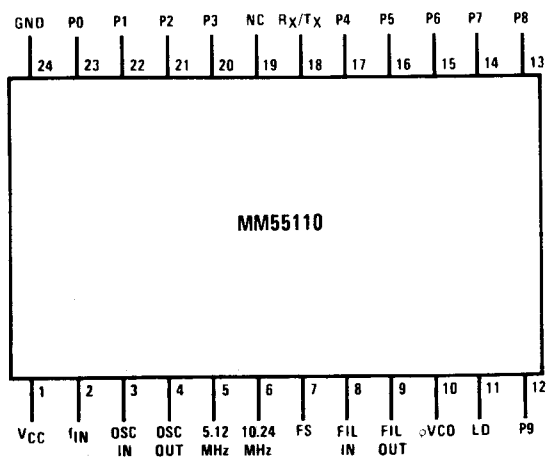
Dual-In-Line Package



TOP VIEW

Order Number MM55108N
See Package 20

Dual-In-Line Package



TOP VIEW

Order Number MM55110N
See Package 22

Pin Descriptions

P0–P9	Programmable Divider Inputs
f_{IN}	Frequency Input From VCO (Mixed down)
OSC IN	Oscillator Amplifier Input
OSC OUT	Oscillator Amplifier Output
LD	Lock Detector
φVCO	Output of Phase Detector for Control of VCO
FS	Frequency Division Select "1" for 2^{10} Division "0" for 2^{11} Division
5.12 MHz OUT	Buffered 5.12 MHz Output (Oscillator Frequency ÷ By 2)
10.24 MHz OUT	Buffered 10.24 MHz Output (Oscillator Frequency)
FILTER IN	Filter Amplifier Input
FILTER OUT	Filter Amplifier Output
R_X/T_X	Receive/Transmit Input "0" for Transmit Mode (by (N+91))

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