



# LC7385, 7385M

## DTMF Receiver

### Overview

The LC7385, 7385M CMOS DTMF Receiver ICs integrate bandsplit filter and digital decoder functions for the 16 DTMF digits used in touch-tone telephone systems.

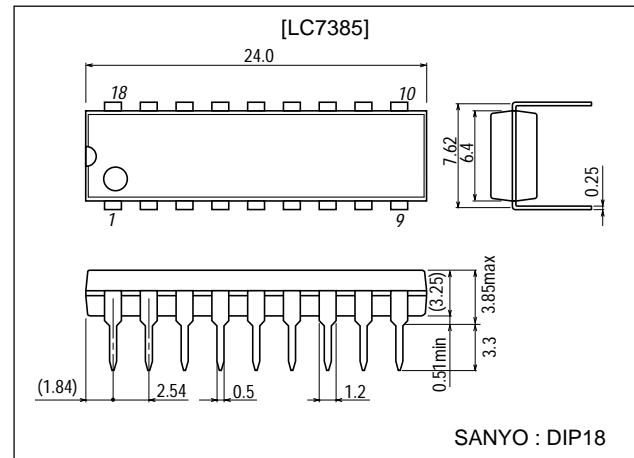
### Features

- Single +5V power supply.
- Decodes all 16 DTMF digits.
- Built-in differential input amplifier.
- On-chip filters, including
  - Dial tone filter.
  - High-group filter.
  - Low-group filter.
- User-selectable acquisition and release times.
- Pin-selectable 4-bit hexadecimal or binary-coded 2-of-8 output.
- 3-state data outputs facilitate microcontroller or other peripheral interfaces.
- Standby mode.
- Low-power double-poly CMOS process.
- LC7385 : 18-pin DIP package.  
LC7385M : 18-pin MFP package.

### Package Dimensions

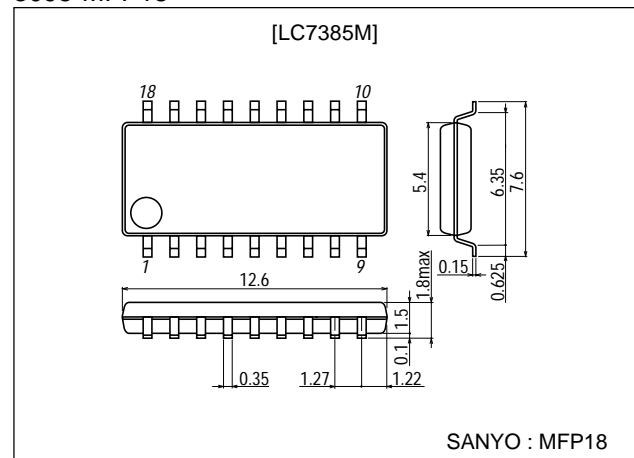
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3007B-DIP18



unit:mm

3095-MFP18

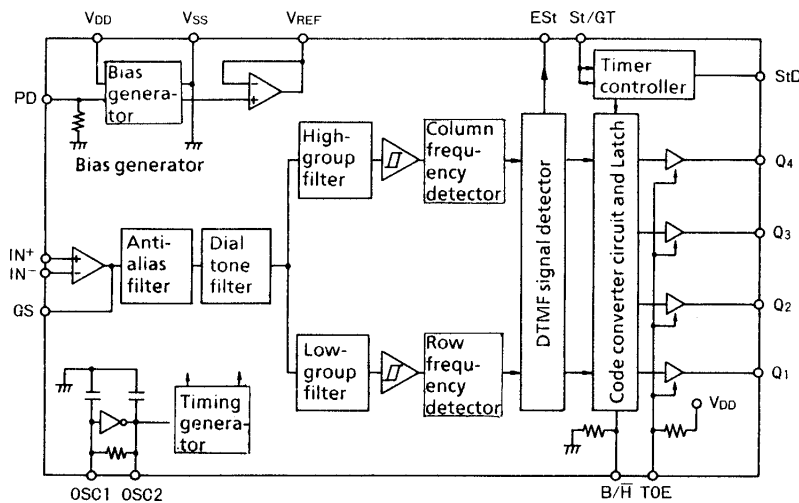


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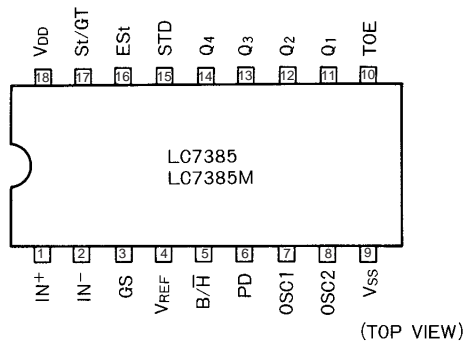
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## Block Diagram



## Pin Assignment



## Pin Functions

Pin No.	Name	I/O	Description
1	IN <sup>+</sup>	I	Input amplifier non-inverting input.
2	IN <sup>-</sup>	I	Input amplifier inverting input
3	GS	O	Input amplifier output.
4	V <sub>REF</sub>	O	Reference voltage output (V <sub>DD</sub> /2)
5	B/ $\bar{H}$	I	Q1 to Q4 output format selection : Binary 2-of-8 when HIGH Hexadecimal when LOW
6	PD	I	Standby mode when set to HIGH
7	OSC1	I	Clock pins. 3.579545MHz crystal is connected between OSC1 and OSC2.
8	OSC2	O	
9	V <sub>SS</sub>		Power supply. Normally 0V.
10	TOE	I	Q1 to Q4 3-state output selection : Enabled when HIGH High-impedance when LOW
11	Q1	O	3-state data output
12	Q2		
13	Q3		
14	Q4		
15	StD	O	Goes HIGH when valid tone pair duration exceeds set guard time.
16	ESt	O	Goes HIGH when valid tone paire is detected.
17	St/GT	I/O	Used to set guard time.
18	V <sub>DD</sub>		Power supply. Normally 5V.

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## Specifications

### Absolute Maximum Ratings at $T_a=25\pm 2^\circ\text{C}$ , $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +7.0	V
Input voltage	$V_{IN}$		-0.3 to $V_{DD}+0.3$	V
Input current	$I_{IN}$		-10 to +10	mA
Output voltage	$V_{OUT}$		-0.3 to $V_{DD}+0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$-40^\circ\text{C}\leq T_a\leq 85^\circ\text{C}$	DIP-18 : 250	mW
			MFP-18 : 180	mW
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-50 to +125	$^\circ\text{C}$

### Allowable Operating Conditions at $T_a=-40$ to $+85^\circ\text{C}$ , $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating voltage	$V_{DD}$		4.75		5.25	V
Input high-level voltage	$V_{IH}$	Pins 6, 10	$0.7V_{DD}$			V
		Pin 5	$0.85V_{DD}$			V
Input low-level voltage	$V_{IL}$	Pins 6, 10			$0.3V_{DD}$	V
		Pin 5			$0.15V_{DD}$	V

Note : When soldering the 18-pin MFP package, solder it manually or use the infrared reflow method.

Do not use the dip-soldering method. The conditions for the infrared reflow method are  $235^\circ\text{C}$  max., 10s.

### DC Electrical Characteristics at $T_a=25\pm 2^\circ\text{C}$ , $V_{DD}=5\text{V}$ , $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply current	$I_{DD(op)}$			3.0	7.0	mA
Standby supply current	$I_{DD(st)}$	$PD=5V$			100	$\mu\text{A}$
Output high-level current	$I_{OH}$	$V_{OUT}=4.6\text{V}$ , pins 11, 12, 13, 14, 15, 16		-0.8	-0.4	mA
		$V_{OUT}=4.6\text{V}$ , pin 17		-3.0	-1.2	mA
Output low-level current	$I_{OL}$	$V_{OUT}=0.4\text{V}$ , pins 11, 12, 13, 14, 15, 16	1.0	2.5		mA
		$V_{OUT}=0.4\text{V}$ , pin 17	1.2	3.0		mA
OFF-state output current	$I_{OZH}$ $I_{OZL}$	$TOE=0\text{V}$ , $V_{OUT}=5\text{V}$ , pins 11, 12, 13, 14			10	$\mu\text{A}$
		$TOE=0\text{V}$ , $V_{OUT}=5\text{V}$ , pins 11, 12, 13, 14	-10			$\mu\text{A}$
Input high-level current	$I_{IH}$	$V_{IN}=5\text{V}$ , pins 1, 2, 10			10	$\mu\text{A}$
Input low-level current	$I_{IL}$	$V_{IN}=0\text{V}$ , pins 1, 2, 5, 6	-10			$\mu\text{A}$
Pull-up (source) current	$I_{SO}$	$TOE=0\text{V}$ , pin 10	-15	-5		$\mu\text{A}$
Pull-down (sink) current	$I_{SI}$	$PD, B/H=5\text{V}$ , pins 5, 6		5	15	$\mu\text{A}$
St/GT threshold voltage	$V_{TST}$	Pin 17		2.35		V
$V_{REF}$ output voltage	$V_{REF}$	No load, pin 4	2.4		2.7	V
$V_{REF}$ output resistance	$R_{REF}$	Pin 4		1		k $\Omega$

### Input Amplifier Characteristics at $T_a=25\pm 2^\circ\text{C}$ , $V_{DD}=5\text{V}$ , $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input offset voltage	$V_{IO}$		-25		+25	mV
Input offset current	$I_{IO}$	$V_{SS}\leq V_{IN}\leq V_{DD}$		$\pm 100$		nA
Power supply rejection	PSRR	1kHz		60		dB
Common mode rejection	CMRR			60		dB
Open-loop voltage gain	$A_O$			65		dB
0dB Gain Bandwidth	$f_T$			1.5		MHz
Maximum output voltage	$V_O$	$R_L\geq 100\text{k}\Omega$		4.5		Vp-p
Tolerable capacitive load	$C_L$			100		pF
Tolerable resistive load	$R_L$			50		k $\Omega$
Common mode range	$V_{CM}$	No load		3.0		Vp-p

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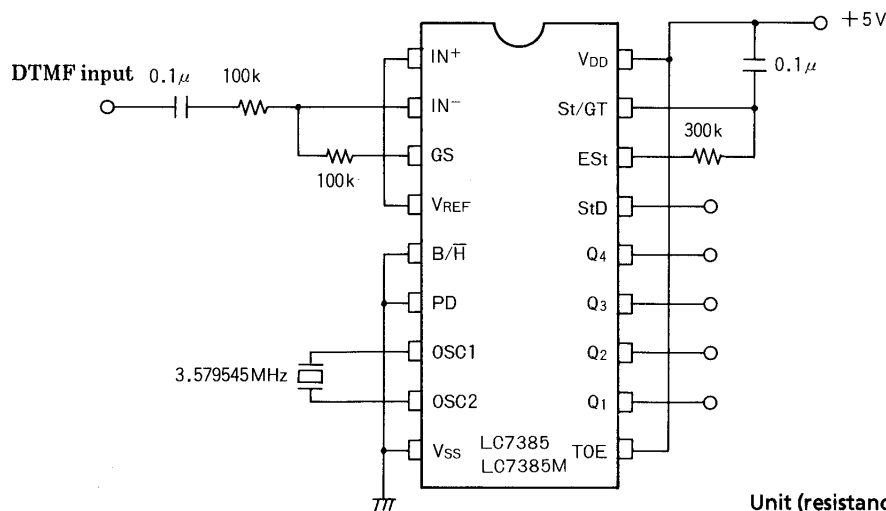
**AC Characteristics** at  $T_a=25\pm 2^\circ\text{C}$ ,  $V_{DD}=5\text{V}$ ,  $V_{SS}=0\text{V}$ ,  $f_{OSC}=3.579545\text{MHz}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Valid input signal level		1, 2, 3, 5, 6, 9	-29		1.1	dBm
Twist accept limit		2, 3, 6, 9, 11		$\pm 10$		dB
Frequency deviation accept limit		2, 3, 5, 9			$\pm 1.5\%$ $\pm 2\text{Hz}$	
Frequency deviation reject limit		2, 3, 5	$\pm 3.5$			%
Third tone tolerance		2, 3, 4, 5, 9, 10		-16		dB
Dial tone tolerance		2, 3, 4, 5, 8, 9, 10		+18		dB
Noise tolerance		2, 3, 4, 5, 7, 9, 10		-12		dB
Tone present detection time	$t_{DP}$	See timing diagram.	5	11	14	ms
Tone absent detection time	$t_{DA}$		0.5	4.0	8.5	ms
Tone duration accept	$t_{REC}$	Adjustable. See guard time adjustment.	40			ms
Tone duration reject	$t_{REJ}$				20	ms
Interdigit pause accept	$t_{ID}$		40			ms
Interdigit pause reject	$t_{DO}$				20	ms
Propagation delay (St $\rightarrow$ Q)	$t_{PQ}$	TOE=5V, No load		8	11	$\mu\text{s}$
Propagation delay (St $\rightarrow$ StD)	$t_{PSTD}$	TOE=5V, No load		12		$\mu\text{s}$
Output data set-up (Q $\rightarrow$ StD)	$t_{QSTD}$	TOE=5V, No load		4.5		$\mu\text{s}$
Output enable delay	$t_{PTE}$	$R_L=10\text{k}$ , $C_L=50\text{pF}$		50	100	ns
Output disable delay	$t_{PTD}$	$R_L=10\text{k}$ , $C_L=50\text{pF}$		300		ns
Clock frequency	$f_{OSC}$		3.5759	3.5795	3.5831	MHz
Clock capacitive load	$C_{XO}$	OSC2			30	pF

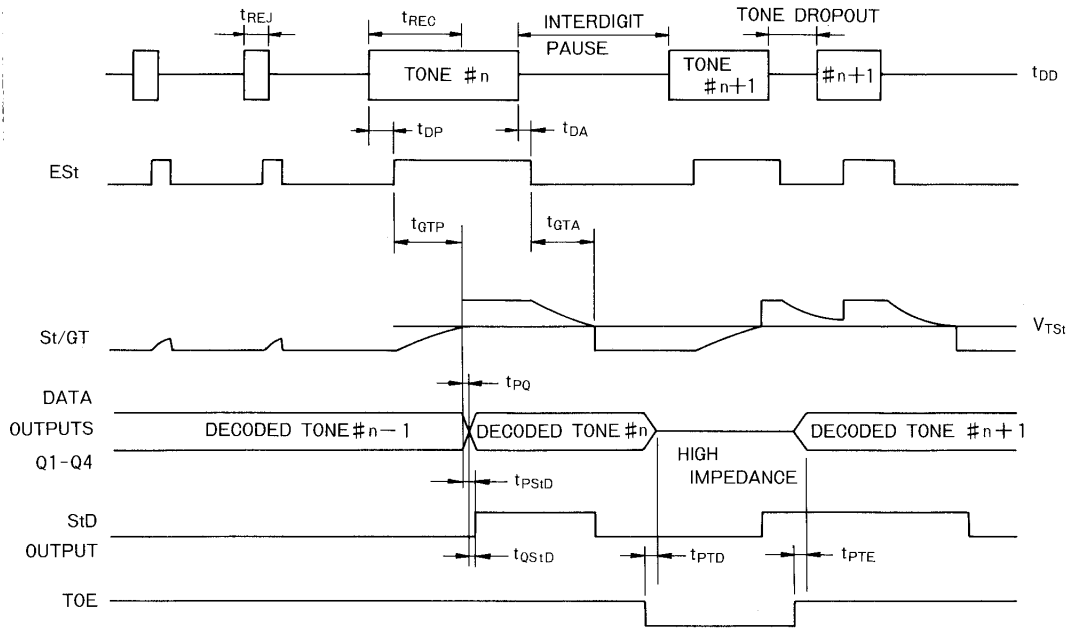
## Conditions

1. dBm=decibels above or below a reference power of 1mW into a 600 $\Omega$  load.
2. All 16 DTMF tones.
3. 40ms DTMF tone duration and 40ms pause duration.
4. Nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair deviated by  $\pm 1.5\%$   $\pm 2\text{Hz}$ .
7. Bandwidth limited (0 to 3kHz) Gaussian noise.
8. 350Hz and 440Hz +2% dial tone frequencies.
9. Error rate better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Twist=ratio of high-frequency tone level to low-frequency tone level.

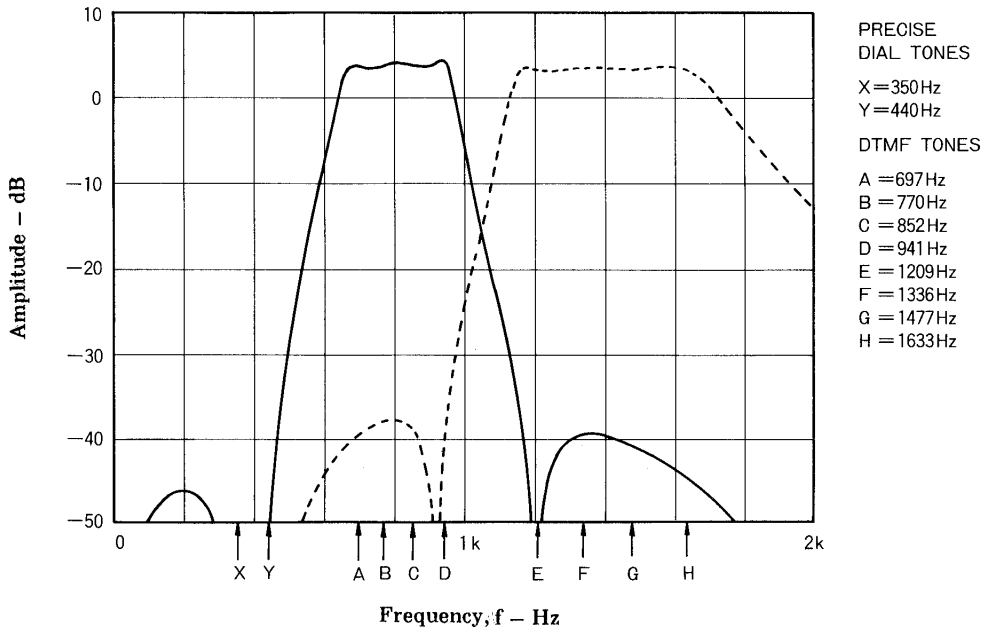
## Single-Ended Input Configuration



Timing Diagram



Typical Filter Characteristics



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## Decode Table

FL	FH	KEY	TOE	B/F="L"				B/F="H"			
				Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1
697	1209	1	H	L	L	L	H	L	L	L	L
697	1336	2	H	L	L	H	L	L	L	L	H
697	1477	3	H	L	L	H	H	L	L	H	L
770	1209	4	H	L	H	L	L	L	H	L	L
770	1336	5	H	L	H	L	L	L	H	L	H
770	1477	6	H	L	H	H	L	L	H	H	L
852	1209	7	H	L	H	H	H	H	L	L	L
852	1336	8	H	H	L	L	L	H	L	L	H
852	1477	9	H	H	L	L	L	H	L	H	L
941	1336	0	H	H	L	H	L	H	H	L	H
941	1209	*	H	H	L	H	H	H	H	L	L
941	1477	#	H	H	H	L	L	H	H	H	L
697	1633	A	H	H	H	L	L	L	L	H	H
770	1633	B	H	H	H	H	L	L	H	H	H
852	1633	C	H	H	H	H	H	H	L	H	H
941	1633	D	H	L	L	L	L	H	H	H	H
-	-	-	L	Z	Z	Z	Z	Z	Z	Z	Z
								ROW m		COL n	

Note : Z=High impedance

## DTMF Dialing Matrix

	C1	C2	C3	C4
R1	1	2	3	A
R2	4	5	6	B
R3	7	8	9	C
R4	*	0	#	D

## Guard Time Setting

Component values are chosen using the following formula :

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

(a) Basic Circuit

$$t_{GTP} = RC \cdot \ln [V_{DD}/(V_{DD} - V_{TST})]$$

$$t_{GTA} = RC \cdot \ln (V_{DD}/V_{TST})$$

(b)  $t_{GTP} < t_{GTRA}$

$$t_{GTP} = R_1 R_2 / (R_1 + R_2) \cdot C \cdot \ln [V_{DD}/(V_{DD} - V_{TST})]$$

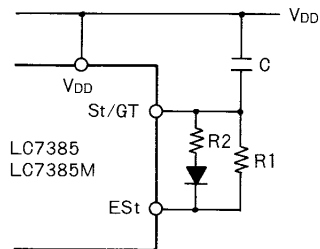
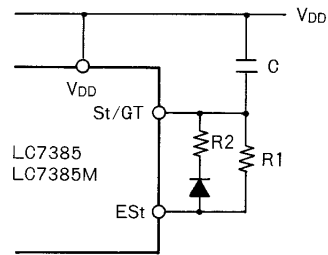
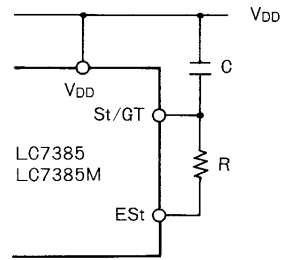
$$t_{GTA} = R_1 C \cdot \ln (V_{DD}/V_{TST})$$

(c)  $t_{GTP} > t_{GTA}$

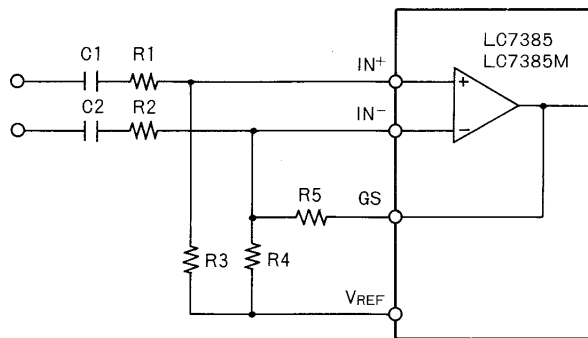
$$t_{GTP} = R_1 C \cdot \ln [V_{DD}/(V_{DD} - V_{TST})]$$

$$t_{GTA} = R_1 R_2 / (R_1 + R_2) \cdot C \cdot \ln (V_{DD}/V_{TST})$$

## Guard Time Adjustment



## Differential Input Configuration



## Example of component values

$$C_1 = C_2 = 0.01 \mu\text{F}$$

$$R_1 = R_2 = R_5 = 100 \text{k}\Omega$$

$$R_4 = 60 \text{k}\Omega, R_3 = 37.5 \text{k}\Omega$$

$$R_3 = \frac{R_4 R_5}{R_4 + R_5}$$

**Voltage gain :**  $AV = \frac{R_5}{R_1}$

**Input impedance=**  $2 \sqrt{R_1^2 + \left(\frac{1}{2\pi f C_1}\right)^2}$

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