

MSM2128RS

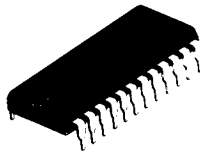
2 KW x 8 BIT STATIC RAM

GENERAL DESCRIPTION

The OKI MSM2128 is a 16384 bits static Random Access Memory organized as 2048 words by 8 bits using Advanced N-channel Silicon Gate MOS technology. It uses fully static circuitry throughout and no clocks or refresh are required. The reduced standby power dissipation is automatically performed by CS control. Single +5 V Power supply. All inputs and outputs are directly TTL compatible. Common data I/O using three-state outputs. The 24 pin package is pin compatible with standard 16 K UV Erasable Programmable ROM.

FEATURES

- Single power supply . . . MSM2128-12RS
- External clock and refresh operation not required . . . 660 mW (max)
- Access time
 - MSM2128-12RS . . . 120ns (max)
 - MSM2128-15RS . . . 150ns (max)
 - MSM2128-20RS . . . 200ns (max)
- Low power dissipation
 - during operation . . . MSM2128-15RS/20RS
 - . . . 550 mW (max)
- TTL compatible I/O
- Three-state I/O
- Common data I/O capability
- Power down mode using chip select signal
- Convertibility of pins used in 16KEPROM MSM2716



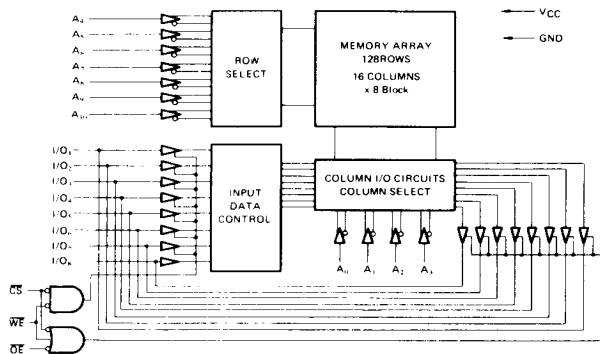
PIN CONFIGURATION

(Top View)

A ₁₅	1	24	V _{CC}
A ₁₄	2	23	A ₀
A ₁₃	3	22	A ₁
A ₁₂	4	21	WE
A ₁₁	5	20	OE
A ₁₀	6	19	A ₁₀
A ₉	7	18	CS
A ₈	8	17	I/O ₀
I/O ₁	9	16	I/O ₁
I/O ₂	10	15	I/O ₂
I/O ₃	11	14	I/O ₃
V _{SS}	12	13	I/O ₄

A₀~A₁₀: Address Inputs
 I/O₀~I/O₇: Data Input/Output
 V_{CC}: Power (5V)
 V_{SS}: Ground
 WE: Write Enable
 CS: Chip Select
 OE: Output Enable

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	-0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_{IN}	-0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	-55 to 150	°C	
Power Dissipation	P_D	1.0	W	

DC AND OPERATING CHARACTERISTICS

($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise notes.)

Parameter	Symbol	2128-12RS			2128-15/20RS			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Load Current	I_{LI}	-10		10	-10		10	μA	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND to } V_{CC}$
Output Leakage Current	I_{LO}	-10		10	-10		10	μA	$\overline{CS} = \overline{OE} = V_{IH}$, $V_{CC} = \text{Max.}$ $V_{out} = \text{GND to } V_{CC}$
Operating Current	I_{CC}			120			100	mA	$V_{CC} = \text{Max.}$ $\overline{CS} = V_{IL}$ $I_{I/O} = 0 \text{ mA}$ $t_{cyc} = \text{Min.}$
Standby Current	I_{SB}			15			15	mA	$V_{CC} = \text{Min. to Max.}$ $\overline{CS} = V_{IH}$
Peak Power-on Current	I_{SBP}			20			20	mA	$V_{CC} = \text{GND to } V_{CC} = \text{Min.}$ $\overline{CS} = \text{Lower of } V_{CC}$ or V_{IH}
Input Voltage	V_{IH}	2	5	6	2	5	6	V	Respect to V_{SS}
	V_{IL}	-0.5	0	0.8	-0.5	0	0.8	V	
Output Voltage	V_{OH}	2.4		V_{CC}	2.4		V_{CC}	V	$I_{OH} = -1.0 \text{ mA}$
	V_{OL}			0.4			0.4	V	$I_{OL} = 2.1 \text{ mA}$

Notes 1. Typical limits are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, and specified loading.

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AC CHARACTERISTICS

($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted.)

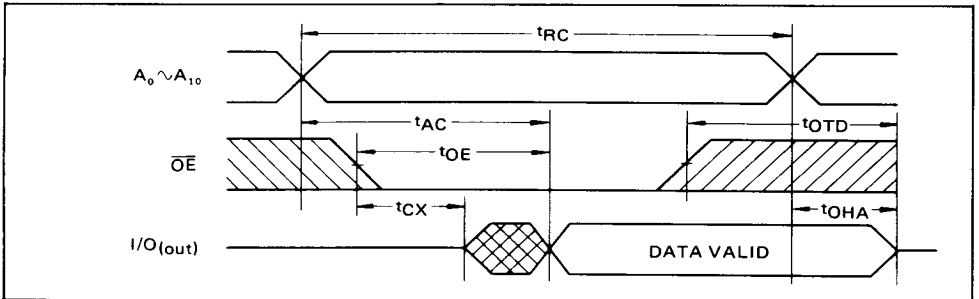
AC TEST CONDITIONS

Parameter	Conditions
Input High Level	2.0V
Input Low Level	0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	$C_L = 100 \text{ pF}$, 1TTL Gate

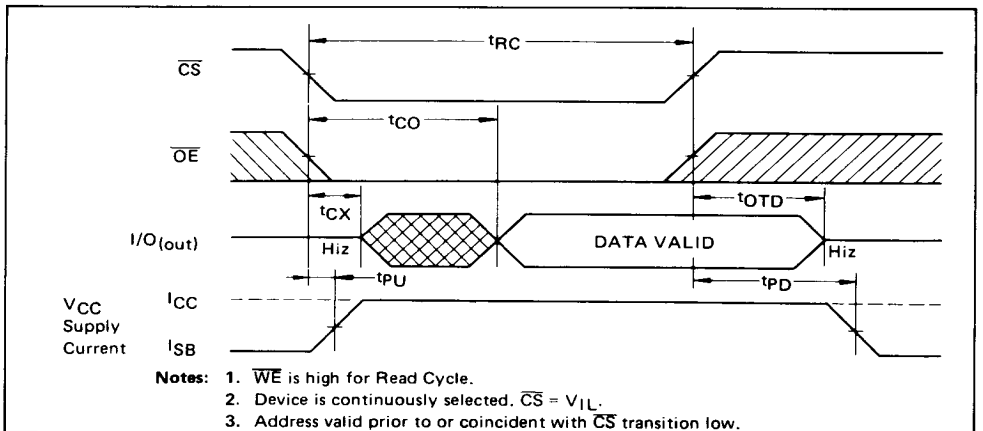
READ CYCLE ⁽¹⁾

Parameter	Symbol	2128-12RS		2128-15RS		2128-20RS		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t _{RC}	120		150		200		ns	
Address Access Time	t _{AC}		120		150		200	ns	
Output Enable to Output Delay	t _{OE}		50		60		70	ns	
Chip Select Access Time	t _{CO}		120		150		200	ns	
Chip Selection to Output in Low Z	t _{CX⁽²⁾}	10		10		10		ns	
Chip Selection to Output in High Z	t _{OTD⁽³⁾}	0	40	0	50	0	60	ns	
Output Hold from Address Time	t _{OHA}	10		10		10		ns	
Chip Select to Power Up Time	t _{PU}	0		0		0		ns	
Chip Select to Power Down Time	t _{PD}		50		60		80	ns	

READ CYCLE NO. 1 ⁽⁸⁾ ⁽⁹⁾



READ CYCLE NO. 2 ⁽⁸⁾ ⁽¹⁰⁾

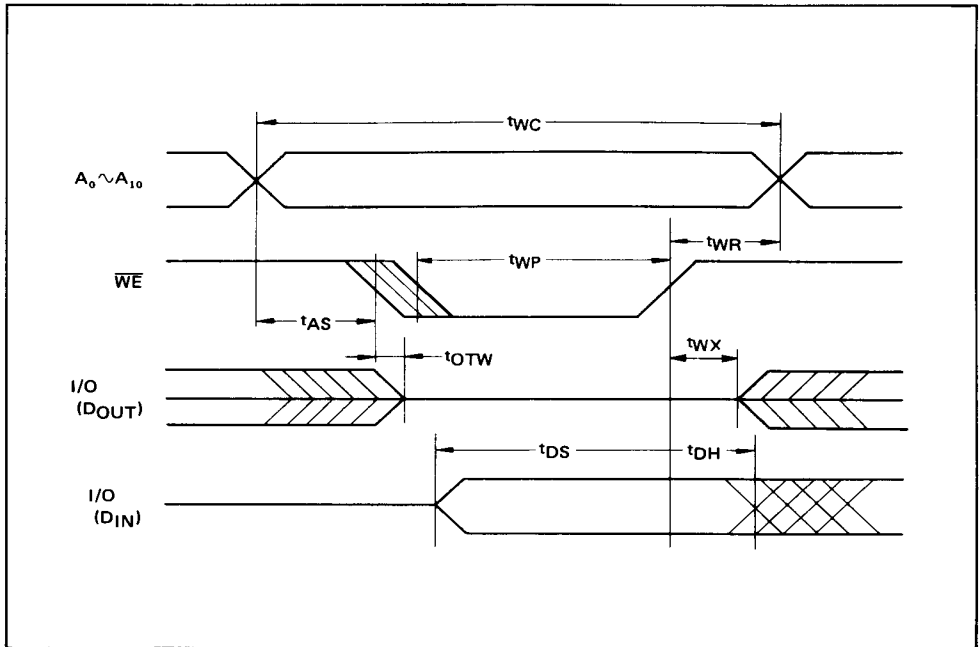


WRITE CYCLE (4) (5)

Parameter	Symbol	2128-12RS		2128-15RS		2128-20RS		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	120		150		200		ns	
Chip Selection to End of Write	t_{CW}	90		120		150		ns	
Address Setup Time	t_{AS}	20		20		20		ns	
Write Pulse Width	t_{WP}	60		80		100		ns	
Write Recovery Time	$t_{WR}^{(6)}$	10		10		10		ns	
Data Valid to End of Write	$t_{DS}^{(6)}$	50		70		90		ns	
Data Hold Time	$t_{DH}^{(6)}$	10		15		15		ns	
Write Enabled to Output in High Z	$t_{OTW}^{(7)}$	0	40	0	50	0	60	ns	
Output Active from End of Write	t_{WX}	5		5		5		ns	

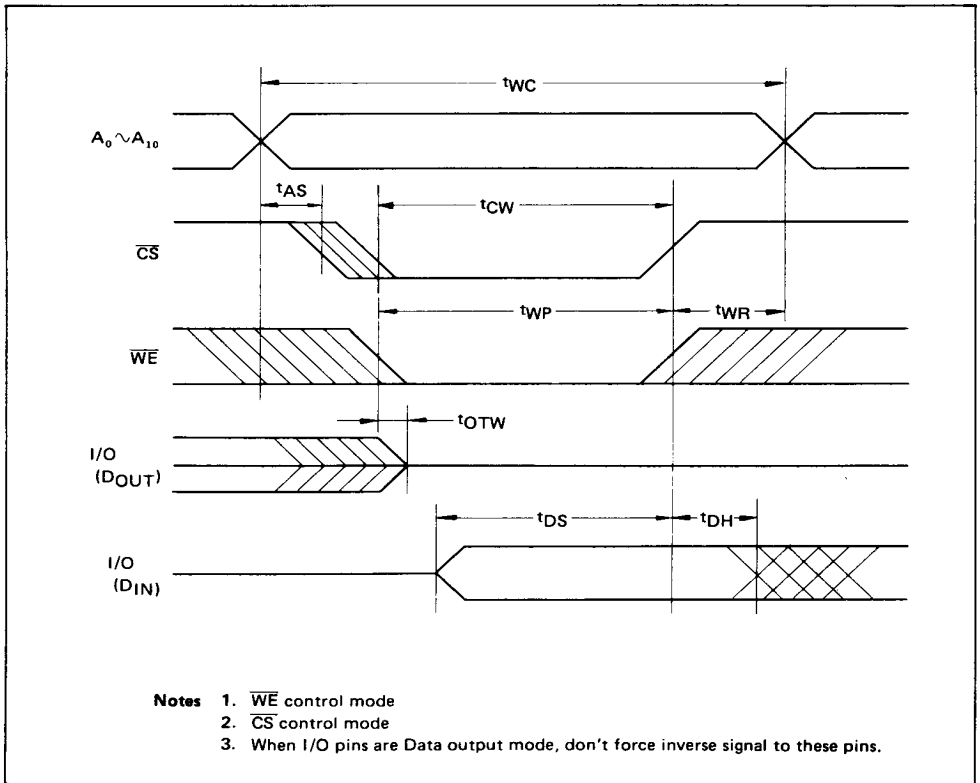
- Notes**
1. A read occurs during the overlap of a low \overline{CS} , a low \overline{OE} and a high \overline{WE} .
 2. t_{CX} is specified from \overline{CS} or \overline{OE} , whichever occurs last.
 3. t_{OTD} is specified from \overline{CS} or \overline{OE} , whichever occurs first.
 4. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} .
 5. \overline{OE} may be allowed in a Write Cycle both high and low.
 6. t_{WR} , t_{DS} , and t_{DH} are specified from \overline{CS} or \overline{WE} , whichever occurs first.
 7. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.

WRITE CYCLE NO. 1⁽¹¹⁾ (13)



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WRITE CYCLE NO. 2⁽¹²⁾ (13)



FUNCTION TRUTH TABLE

CS	WE	OE	Mode	Output	Power
H	X	X	Not Selected	High Z	Standby
L	L	X	Write	High Z	Active
L	H	L	Read	DOUT	Active
L	H	H	Not Selected	High Z	Active

CAPACITANCE

($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min.	Max.	Unit	Conditions
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O} = 0\text{V}$
Input Capacitance	C_{IN}		6	pF	$V_{IN} = 0\text{V}$

Note: This parameter is periodically sampled and not 100% tested.